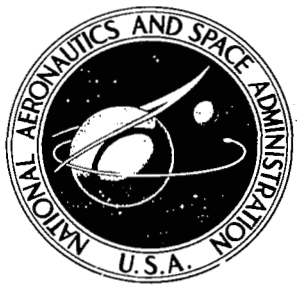
NASA CONTRACTOR REPORT



NASA CR-1346

RELIABILITY HANDBOOK FOR SILICON MONOLITHIC MICROCIRCUITS

Volume 1 — Application of Monolithic Microcircuits

by William C. Weger, et al.

Prepared by
TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas
for George C. Marshall Space Flight Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • APRIL 1969

RELIABILITY HANDBOOK FOR

SILICON MONOLITHIC MICROCIRCUITS

Volume 1 - Application of Monolithic Microcircuits

By William C. Weger, et al.

Issued by Originator as Report No. 03-67-04

Prepared under Contract No. NAS 8-20639 by
TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas

for George C. Marshall Space Flight Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Clearinghouse for Federal Scientific and Technical Information
Springfield, Virginia 22151 – CFSTI price $3.00

FOREWORD

This handbook was prepared as an aid in determining the most effective application, testing, handling, and quality and reliability assurance controls for integrated circuits. It was compiled in two books of two volumes each and deals primarily with the subjects of application, failure mechanisms, failure analysis, and reliability assessment. Some similarity may be noted between NASA CR 1110, "Microelectronic Device Data Handbook," and the data presented herein; however, NASA CR 1110 deals with microcircuits in general, while this document was prepared as a reliability handbook and deals with monolithic microcircuits only.

The effort resulting in the publication of this handbook was produced under the technical direction of the Parts and Microelectronics Technology Branch, Future Programs and Technology Office, Quality and Reliability Assurance Laboratory, George C. Marshall Space Flight Center, Alabama.

D. Grau
Director, Quality and Reliability
Assurance Laboratory

PREFACE

This publication, "Application of Monolithic Microcircuits," is Volume 1 of a four-volume series entitled, "Reliability Handbook for Silicon Monolithic Microcircuits." The Handbook was prepared for the National Aeronautics and Space Administration by Texas Instruments Incorporated, under Contract NAS 8-20639. The Handbook series consists of the following volumes:

Volume 1 Application of Monolithic Microcircuits

Volume 2 Failure Mechanisms of Monolithic Microcircuits

Volume 3 Failure Analysis of Monolithic Microcircuits

Volume 4 Reliability Assessment of Monolithic Microcircuits

The purpose of the Handbook is to provide aid in determining the most effective application and understanding of monolithic microcircuits, and the most effective quality and reliability assurance controls for the circuits.

Volume 1, "Application of Monolithic Microcircuits," describes:

- Typical problems that have been experienced with certain applications and modes of operation for several families of digital microcircuits and linear microcircuits.
- The most reliable and trouble-free methods of use or application of each type of circuit presented here.
- How to obtain maximum information from manufacturers' data sheets.
- A method for derating the devices in actual use, and a method by which to assess the gain (or loss) in circuit performance and reliability which results from the application of the derating method.
- The characteristics, advantages, and disadvantages of the various types of packages now available, and a method by which the user can evaluate the available packages and select the one most suitable for the intended application.
- Methods for the interconnection of packages, and methods of assembly of circuits into components and systems.

The following list of acknowledgements is composed of manufacturers of monolithic microcircuits and publishers of related specifications and data who have granted permission for inclusion of the items of previously published forms, data sheets and specifications which appear herein:

Fairchild Semiconductor, a Division of Fairchild Camera and Instrument Corporation

Motorola Semiconductor Products, Inc.

Radio Corporation of America

Rogers Publishing Company, Inc. a Subsidiary of Cahners Publishing Company, Inc., Publishers of EDN

Signetics Corporation

TABLE OF CONTENTS

VOLUME I

APPLICATION OF MONOLITHIC MICROCIRCUITS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

VOLUME 1

FAILURE ANALYSIS METHODS AND PRODECURES

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

VOLUME I

APPLICATION OF MONOLITHIC MICROCIRCUITS

SECTION I

INTRODUCTION

During the past decade, the circuit designer has gained much greater flexibility through the use of semiconductor devices, enabling him to "design-in" additional product features. Monolithic circuits, even more so, represent an explosion of possibilities for:

- Achievement of extreme savings in overall system cost.
- Reduction in the number of connections.
- Reduction of inventory.
- Great increase in system reliability.
- Improved maintainability.

Today, the prospect of reducing system cost while increasing system reliability and decreasing overall system size is causing a tremendous effect in the consideration of integrated electronics in product design.

Included in "integrated electronics" are many types of microminiature electronic devices, and the leading one within the industry today is the monolithic microcircuit. Monolithic microcircuits are complete electronic subassemblies that contain several active and passive components within a common solid body or substrate.

The first commercially available microcircuit was produced in 1960. Since then, monolithic microcircuits have revolutionized the semiconductor industry. The services of many skillful specialists are required to design, produce, and use the small complex devices. The highly refined process of manufacturing monolithic microcircuits is outlined in the following list and illustrated in Figure 1-1.

- Growth of a single-crystal silicon ingot.
- Slicing the ingot into wafers.
- Polishing and finishing the wafers.
- The multistep process of diffusing the individual components and connecting them into the desired circuit.

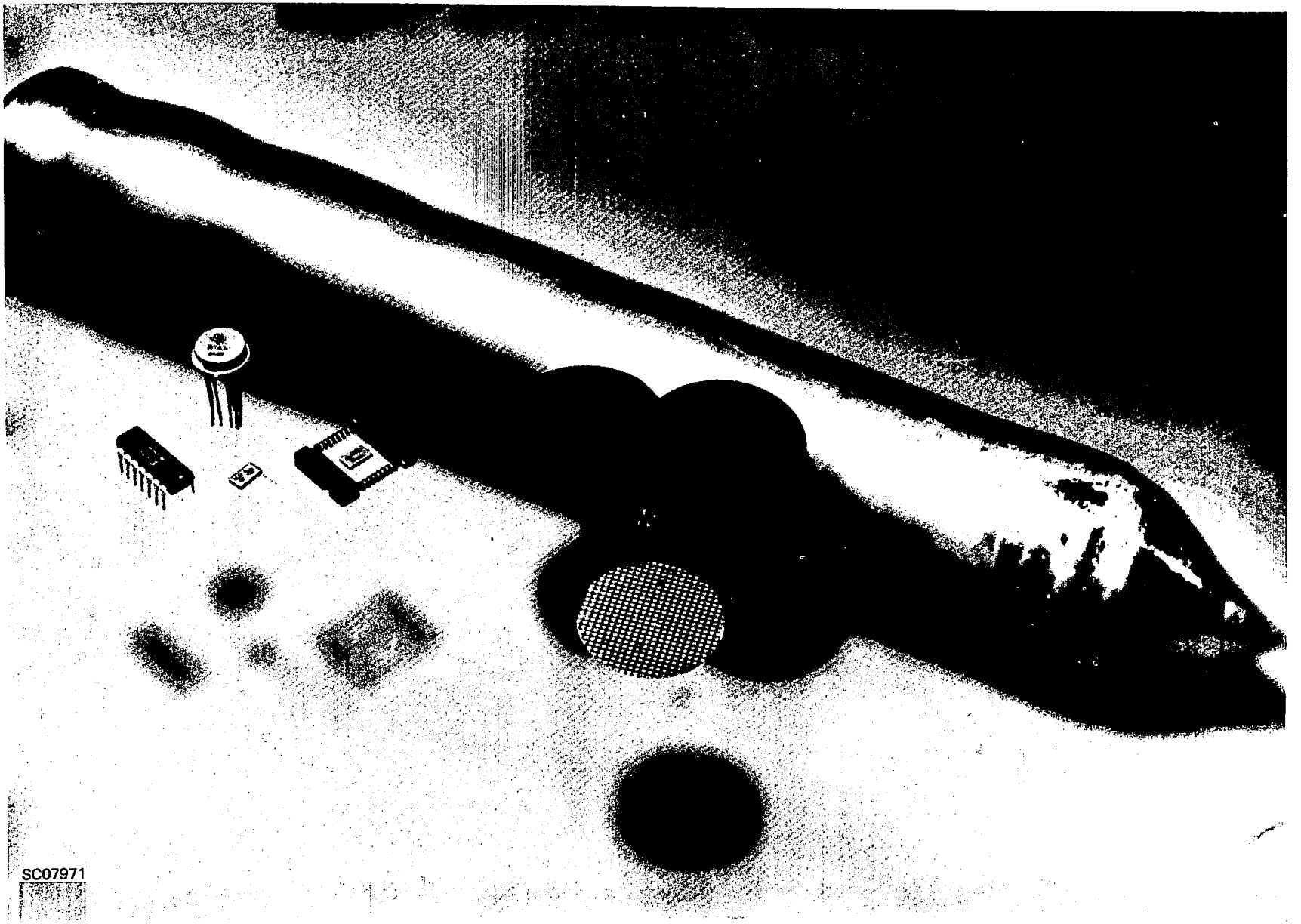


Figure 1-1. An Illustration of the Process Steps in the Manufacture of a Monolithic Microcircuit—from Silicon Ingot to Finished Product

- Separation into individual circuit die.
- Assembling the circuit die into packages.

The individual microcircuit die is very small and is inconvenient to test and handle. The die is therefore encapsulated in some type of housing for protection as well as for ease of handling.

There are two categories of monolithic microcircuits—digital and linear. Digital microcircuits can be divided into a few family groups, such as:

- Resistor-transistor logic (RTL).
- Resistor-capacitor-transistor logic (RCTL).
- Diode-transistor logic (DTL).
- Transistor-transistor logic (TTL).
- Emitter-coupled logic (ECL).

Within the linear category, there are operational and differential amplifiers and differential comparators, plus many possibilities for highly specialized devices. Only the more common amplifiers and comparators will be discussed in this handbook.

In a typical application of monolithic microcircuits, a large portion of the total system consists of packaged microcircuits. Thus, the manufacturer of such a system will acquire a close familiarity with the basic techniques required for successfully designing with monolithic microcircuits. This familiarity, coupled with his own unique methods and refinements, will enable him to achieve an appreciable reduction in design costs, manufacturing costs and checkout time.

This volume of the Handbook will describe:

- Methods used in monolithic construction.
- The available monolithic microcircuit types.
- The available packages for microcircuits.

Application information and selection guides also will be presented.

SECTION II

MONOLITHIC MICROCIRCUIT CONSTRUCTION

A. GENERAL

This part of the Handbook provides descriptions of the fabrication techniques used to manufacture monolithic microcircuits. Also provided is a brief discussion of the basic monolithic microcircuit structures (i. e., triple- and quad-diffused, double epitaxial) and a description of the step-by-step process of diffusion under the epitaxial layer. Then, the characteristics and capabilities of monolithic microcircuit components will be discussed.

B. FABRICATION

The starting point in the manufacture of any semiconductor device is the making of a single crystal of material. For monolithic microcircuits, a silicon crystal is grown by the Czochrolski method. The high purity silicon is placed in a quartz crucible and melted by RF induction heating. Then, a small, specially prepared seed crystal is lowered into the molten silicon and slowly rotated and pulled upward. Under carefully controlled conditions, additional material in the form of a large cylindrical crystal is grown on the seed.

Either during the growing of a single crystal, or later by means of high-temperature solid/gas reactions (diffusion), impurities can be incorporated into the otherwise ordered structure of the single crystal. The crystal is sliced with a diamond saw into many wafers, each a few thousandths of an inch thick. Each crystal contains from 10 to 100 wafers. Each wafer has the potential for being subdivided into 100 to 600 individual circuits 40 to 60 mils square. The wafers, or slices, are then lapped flat by using a very fine grit abrasive, and then chemically etched to form a finished wafer that has an extremely smooth surface.

The most popular basic process for the manufacture of monolithic microcircuits is planar oxide-masked diffusion. The various steps in this process will now be described.

1. Oxidation

An inert, stable layer of silicon dioxide (SiO_2) is grown on the previously described silicon wafer. This is accomplished by placing the silicon wafer in an oxidizing atmosphere at an elevated temperature. The oxide, composed of atoms from the silicon substrate and oxygen atoms from the oxidizing media, acts as a protective coating for the clean bulk silicon. Since one of the basic requisites for semiconductor reliability is an uncontaminated silicon surface, the oxidation represents a very important part of monolithic microcircuit fabrication. Numerous cleaning steps are incorporated during the process to maintain the cleanliness of the wafer.

2. Oxide Removal

Since SiO_2 will prevent the diffusions of various atoms into silicon, it is necessary to provide access through the oxide for the diffusion to take place. By means of a photolithographic process, definite patterns of "windows" or trenches are cut through the oxide to the silicon substrate. A light-sensitive, plastic-like material is applied uniformly to an oxidized slice. Patterns are formed in the photosensitive material by the action of light exposed through a black and white photographic mask which defines the desired pattern. Material under the transparent areas of the mask is hardened, while material which was under the opaque mask areas, in the shape of the areas to be etched, remains unreacted and susceptible to solvent attack. Washing in a developer solution removes the unreacted plastic-like material, leaving a pattern of SiO_2 surrounded by hardened areas of the photosensitive compound. Exposure to a solution of hydrofloric acid causes the SiO_2 to be dissolved from pattern areas. The SiO_2 beneath the coating remains unchanged. Removal of the protective material with suitable solvents provides an oxidized slice with discrete openings in the oxide to the silicon substrate. This procedure is repeated several times during the manufacture of silicon monolithic microcircuits and is referred to as "1st oxide removal (OR)," "2nd OR," etc.

3. Diffusion

After the pattern areas have been opened in the SiO_2, the wafer is ready for the diffusion of the different N or P areas of the individual components. For example, to diffuse an N-type region in a P-type substrate, the wafer is placed in a high-temperature furnace with a phosphorus oxidizing atmosphere. Phosphorus atoms are diffused in the silicon wafer at the open areas of the SiO_2, and those areas of the wafer protected by SiO_2 are not affected. The same procedure is used to construct a P-type area within a wafer. In this case, the wafer is placed in a high-temperature furnace with a boron-oxidizing atmosphere. Since the diffusion is performed in an oxidizing atmosphere, a new oxide layer is grown over the entire wafer, covering the previous open areas. The wafer is masked and etched after each diffusion, to provide

openings in the oxide for the next diffusion. When scheduling any diffusion step, the subsequent processing step must be considered, since the temperature and time required to diffuse the additional steps will cause further diffusion of the previous steps. Diffusion into the silicon occurs in a horizontal as well as a vertical direction, always leaving the actual PN or NP junction covered by the oxide. It is the protective oxide covering that assures contamination-free, oxide-stabilized junctions.

4. Epitaxy

A gas-phase reaction, called "epitaxy," can be used to deposit silicon on the surface of an exposed silicon single crystal. With proper control, the new deposit will also be single-crystal in orientation and can even be doped during growth. Since the reaction takes place quickly compared to a diffusion, the previously doped region is virtually undisturbed, and a "sharp" transition can be produced by the epitaxy technique.

The process of epitaxial crystal growth is basically one of placing silicon atoms, usually by a chemical reaction, on the surface of a silicon slice at high temperature. The atoms wander about the surface until a suitable nucleation point is found, at which time they orient themselves with respect to the substrate-crystal lattice. In this way, a single crystal film grows with the same orientation as the substrate.

In the standard epitaxial process, silicon is heated in a high-temperature reactor in the presence of hydrogen and silicon tectrachloride. The reaction occurs and a single-crystal silicon layer of the same orientation as the substrate is deposited on the slice. If an impurity is added to the silicon tectrachloride, this will be incorporated in the film, and by adding more or less impurities of different types, P- and N-type layers of different resistivities may be formed.

5. Isolation Techniques

Isolation is a basic concept used in monolithic construction to electrically separate the individual circuit components. The reverse-biased PN junction is the most common method for achieving isolation, but it is somewhat inadequate for high-frequency circuits where junction capacitances become important. The PN junction also tends to suffer from dc effects such as junction leakage, inversion layers, and unwanted transistor and PNPN effects.

In the triple-diffused method, impurities are selectively introduced from one side, thus forming the collector of an isolated transistor. The collector-to-substrate PN junction is kept back-biased during circuit operation to provide isolation from other components.

Several isolation methods are used for the epitaxially fabricated circuits. They consist of diffusing through the epitaxial layer to the substrate, using the same type impurities as the substrate. Although the diffusion method for isolation is widely used, it does not provide complete isolation. Many new techniques for isolation are being investigated; however, most methods are not yet practical for high volume production.

One new isolation method, which will be discussed, is shown in Figure 1-2. The dielectric isolation uses a thin layer of SiO_2 to provide isolation between components and substrate. A high concentration of N-type impurities is diffused into the N-type starting material,and this results in an N^+ layer. This N^+ region will ultimately serve to reduce the saturation voltage of the finished devices. Grooves are then etched in the slice to form islands of N^+ covered N-type regions. Next, an oxide is grown over the entire silicon surface, followed by the deposition of a thick polycrystalline silicon layer. This thick (10 mils) polycrystalline layer is lapped to remove any surface irregularities and to furnish a smooth reference plane from which to lap the other side; i. e., the original single-crystal material. Accurately controlled lapping of the single-crystal side will leave islands of the original material, with their buried high-conductivity layer completely isolated from one another by the oxide layer. The polycrystalline material serves merely as a carrier for these islands.

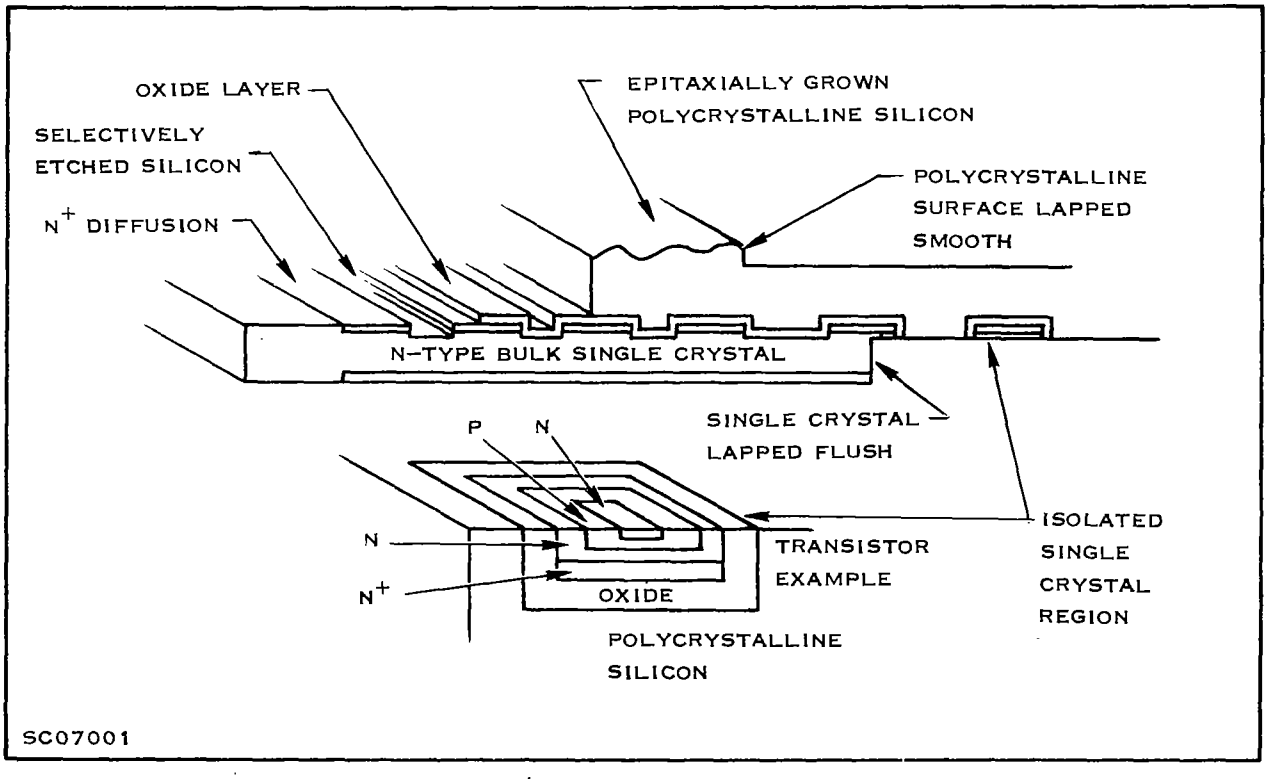


Figure 1-2. Microcircuit Dielectric Isolation

The dielectric-isolation method has its practical limitations, however, par-
ıularly in the degree of sophistication required of the lapping process to adequately
ıntrol the out-diffusion effects mentioned earlier. To provide a reliable circuit, it
important that the circuit designer be aware of the processing difficulties in all
ethods so that a reasonable performance-yield compromise can be reached.

6. Photo Masks

The beginning of the circuit function that is to be produced in monolithic
rm is the design and layout of a group of photographic negatives (photo masks). The
ıotoprocessing of the negatives is a vital part in manufacturing high performance
ımplex microcircuits. It is estimated that a large percentage of all yield losses
·e due either directly or indirectly to photoresist flaws.

The number of steps needed to produce one mask is illustrated in Figure 1-3.
ıe original artwork is accurately fabricated by scribing a commercially available
ndwich of opaque and translucent material. After cutting, the opaque portions are
·ipped off, leaving a replica of the final pattern. This artwork is prepared at 150-
1000 times final size to minimize any possible layout errors and cutting deviations.
e reduction to the final size is accomplished by several photo reduction steps. Ac-
rate step-and-repeat machines are used to lay out many identical patterns to cover
: entire wafer.

In summary, the fabrication of monolithic microcircuits involves two sep-
ate and distinct parts. One part involves the control of the depth and vertical dimen-
ɔns normal to the surface—that is, the circuit process, such as epitaxial layer and
'fusion. The other part involves the layout and design of the photo masks, and the
ide removal process which defines the horizontal dimensions through which the dif-
ɜion (vertical) steps will be accomplished. The interplay between these two parts
the fabrication procedure is illustrated in Figure 1-4.

STRUCTURES

1. General

There are several basic structure types that are used in the fabrication of
ɔnolithic microcircuits. They range from the relatively simple triple-diffused
ructure to the more complex epitaxial structures. Five major types of structures
ll be discussed and a comparison of some of their advantages and disadvantages
ll be presented.

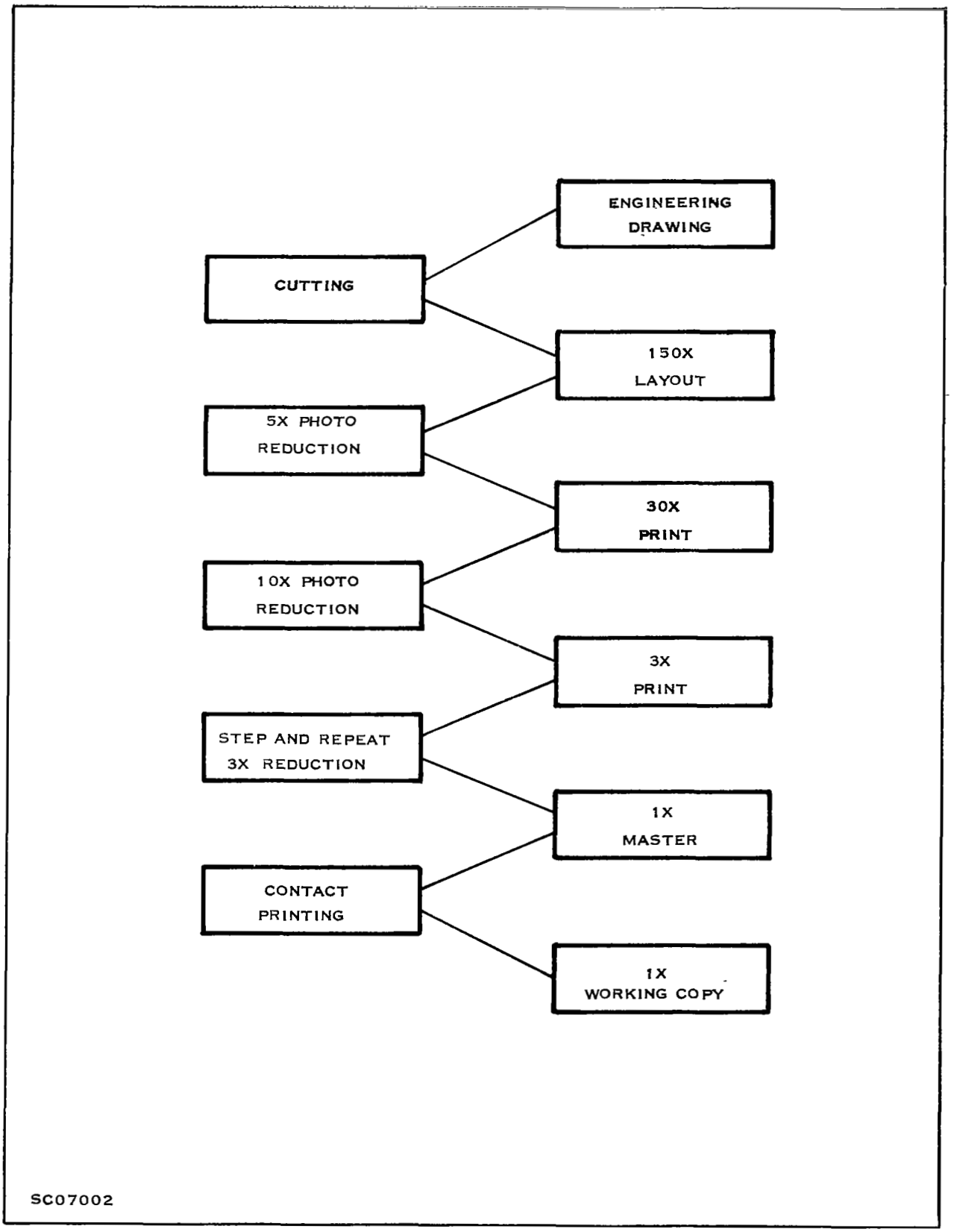
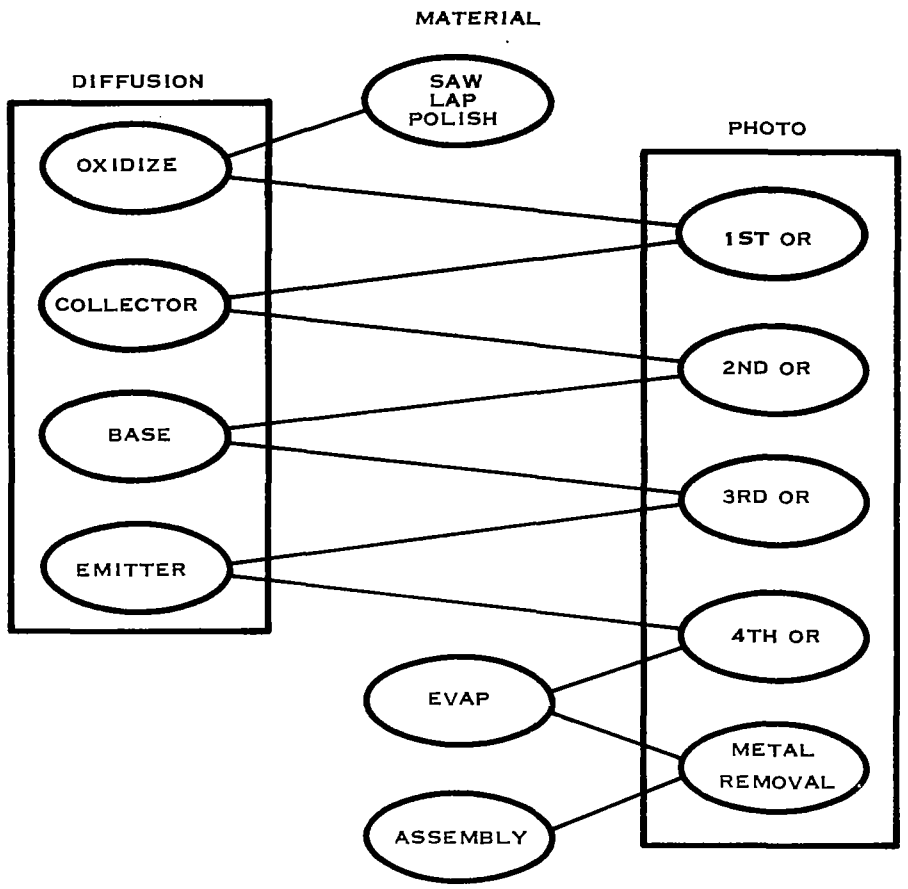


Figure 1-3. Photoreduction Process



3C00049

Figure 1-4. Fabrication Flow of a Monolithic Microcircuit

2. Triple Diffused

The triple-diffused structure was the first planar type used to build microcircuits. The process consists of three sequential diffusion cycles. For the first cycle, a silicon dioxide layer is grown on a P-type substrate. The dioxide layer is selectively etched to provide openings for the collector diffusion. Then, the wafer is subjected to an N-type diffusion to form the collector region for transistors, as well as isolation regions for resistors, diodes, and capacitors. During the diffusion a new silicon dioxide layer is grown over the entire wafer. Prior to the second diffusion cycle, the new SiO_2 layer is selectively opened to permit diffusion of the P-type base region. The wafer is then subjected to a P-type diffusion. Again the newly grown SiO_2 layer

is opened for diffusion of the emitter region,and the diffusion process is repeated to form the N-type emitter. Once more, openings are etched in the SiO_2 layer to provide contact areas for connecting together the individual components. Then, the entire silicon slice is covered with a metal film by means of a vacuum evaporator. By using photoetching techniques similar to those used for oxide removal, the unwanted metal is removed, leaving a metal interconnecting pattern.

The NPN transistor is shown in Figure 1-5, along with a PNP transistor. In the triple-diffused structure, common collector (substrate) PNP transistors are formed by the first two diffusions of N and P for the PNP base and emitter,respectively.

3. Quad Diffused

The quad-diffused technique is very similar to the triple-diffused technique, except for the addition of another diffusion cycle. By starting with N-type substrate, the quad-diffused technique produces both isolated NPN and isolated PNP transistors (Figure 1-6).

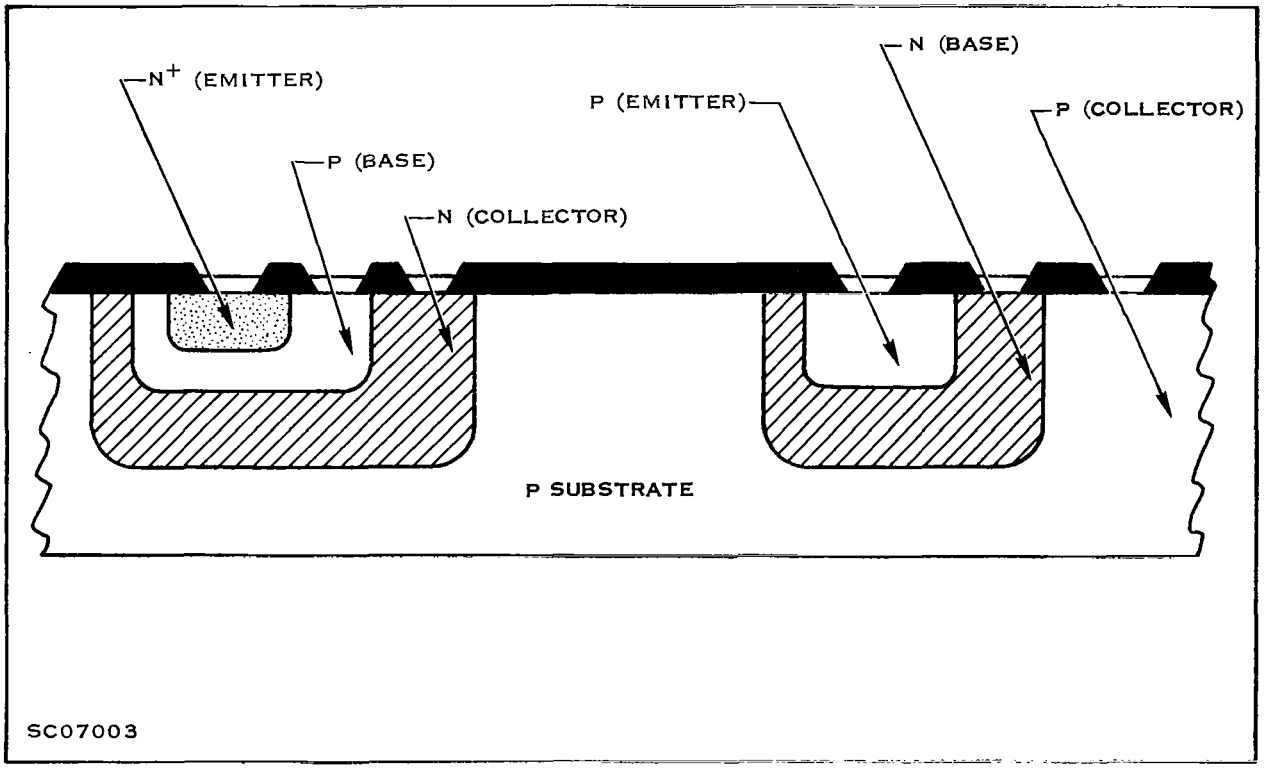


Figure 1-5. Triple-diffused Structure

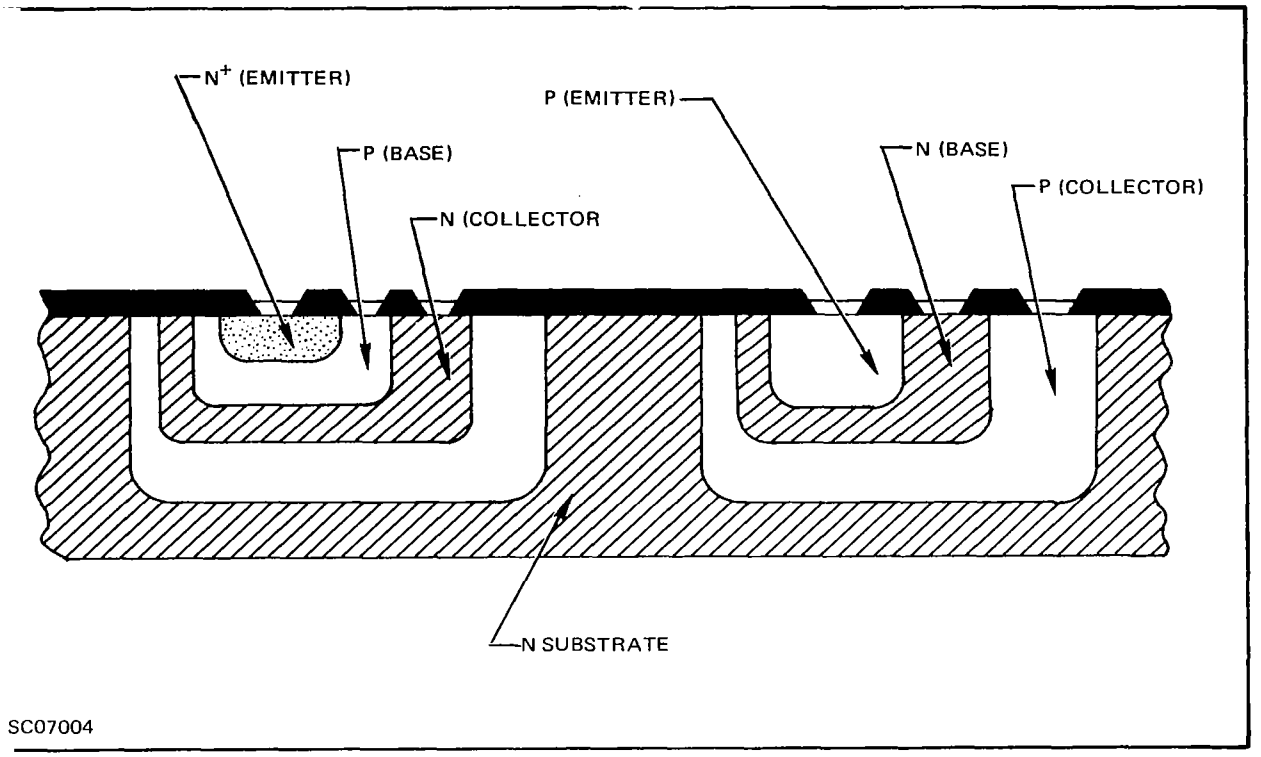


Figure 1-6. Quad-diffused Structure

4. Single-Epitaxial Film

The simplest of the epitaxial transistor structures is the single-epitaxial film. Isolated NPN transistors are formed by first growing an N-type epitaxial film on a P-type substrate, diffusing a deep P-type ring through the N film to isolate the transistor, and making two successive diffusions for P-type base and N-type emitter (Figure 1-7). Transistors formed using this process have significantly lower R_{CS} than that obtained with the triple-diffused process. This results because the epitaxial collector has fairly constant N-dopant concentration across its entire depth, whereas the triple-diffused collector has fairly high N-concentration at the surface but is considerably lower at the base-collector junction.

5. Double-Epitaxial Film

The double-epitaxial structure is very similar to the single-epitaxial structure, except that an N^+ film is grown on the P-type substrate and then an N-type layer is grown on the N^+ layer (Figure 1-8). Isolation of the components is provided by deep-diffusing a P-type ring to the P substrate, through both the N and N^+ films. A P-base and an N^+ emitter are successively diffused into the isolated collector region. An N^+ area is also diffused at the collector contact area to penetrate the top N-film and make contact to the N^+ film. The double-epitaxial technique produces transistors

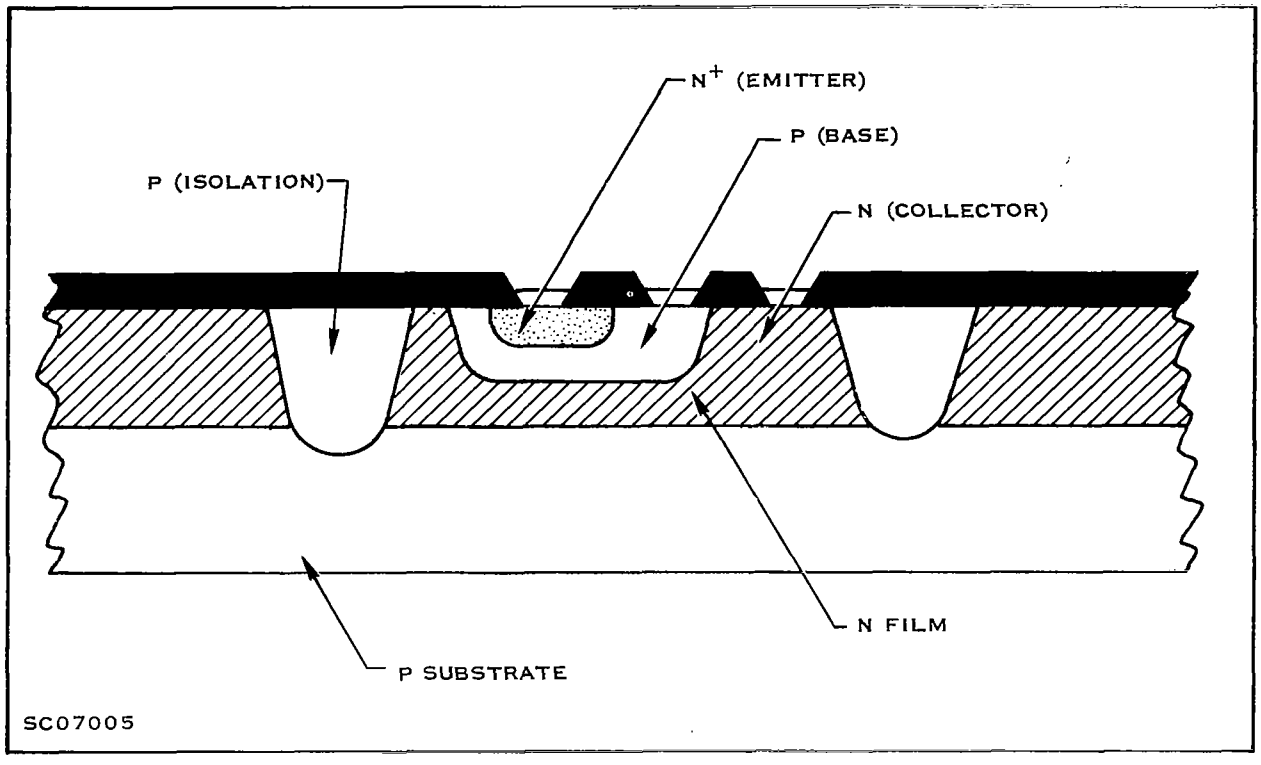


Figure 1-7. Single-Epitaxial Structure

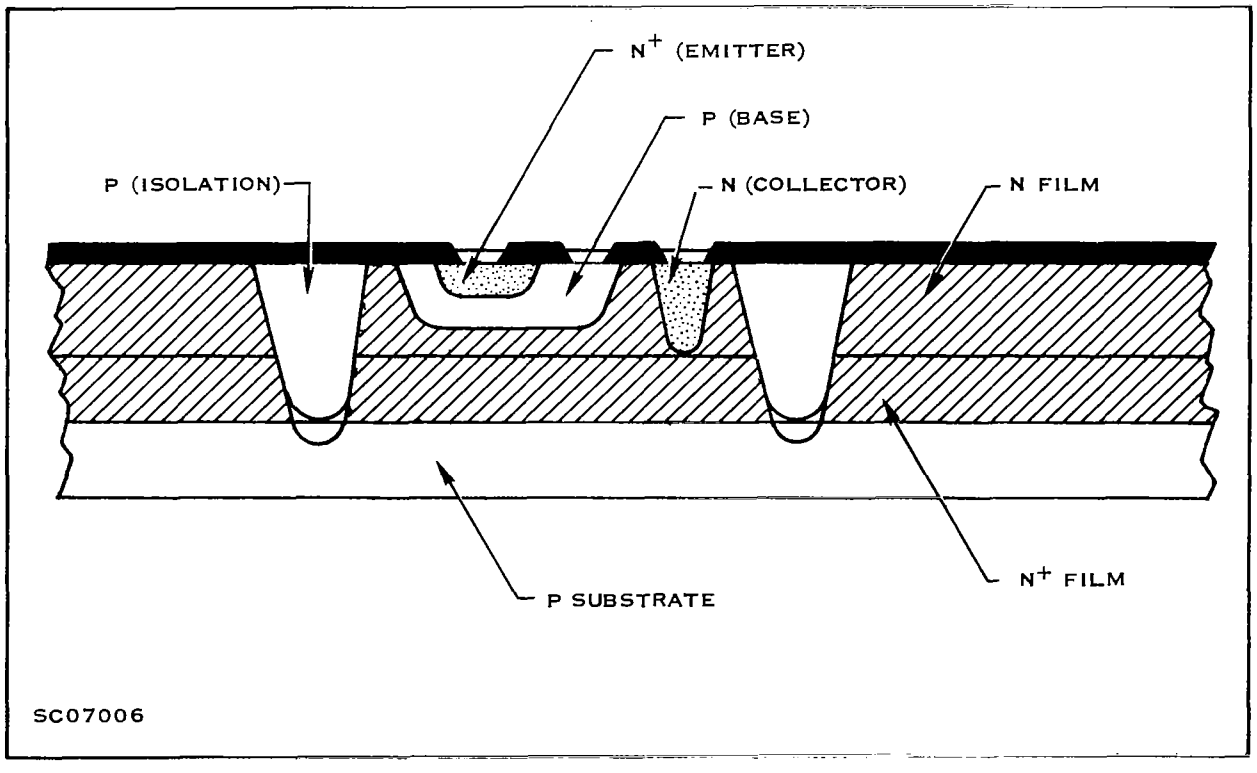


Figure 1-8. Double-Epitaxial Structure

with a lower R_{CS} than the single-epitaxial technique. However, the double-epitaxial process requires a very deep P-isolation diffusion through the two epitaxial layers. This is time-consuming, and due to the wide isolation region, it increases the necessary bar size.

6. Diffusion Under Epitaxial Film

a. General

The diffusion-under-the-epitaxial-film (DUF) process is essentially the same as the double-epitaxial process, except that the N^+ region is diffused into the affected regions instead of growing an N^+ epitaxial layer. The DUF process is becoming widely used in large-scale production of monolithic microcircuits. To illustrate the manufacture of silicon monolithic microcircuits, the fabrication of the simple circuit shown in Figure 1-9 will be discussed, using the DUF process as the basic structure type.

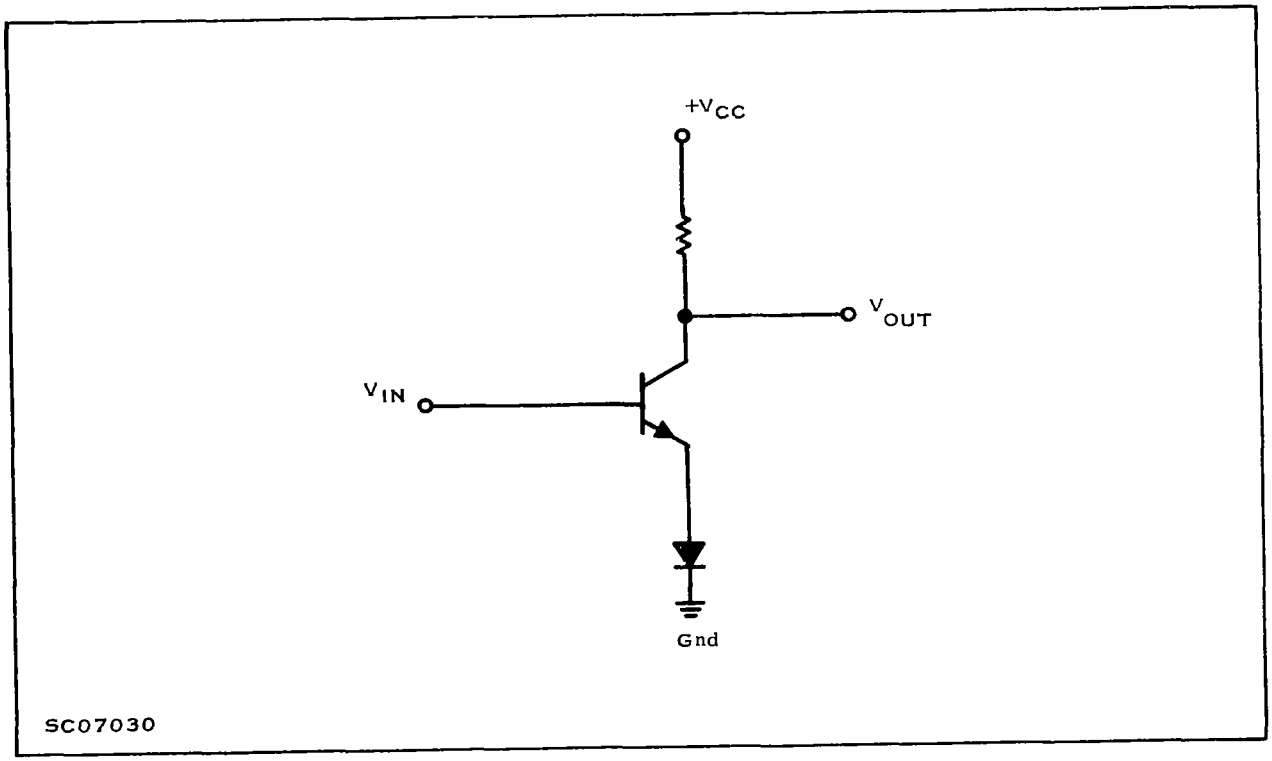


Figure 1-9. Simple Circuit that Illustrates Design and Fabrication by the DUF Process

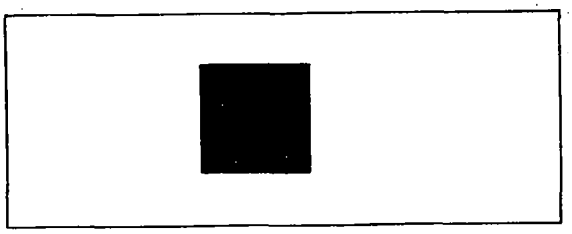
b. Fabrication of a Simple Circuit

After the desired circuit has been designed, a photographic mask is prepared for each of the required manufacturing steps. A set of masks needed for fabrication of the circuit of Figure 1-9 is shown in Figure 1-10. (Actually, these masks are reproduced for each circuit on the wafer.) The shaded portion represents areas of the oxide or metal that will be chemically removed, whereas, the light areas will be covered with photoresist material and will not be removed during the etching process.

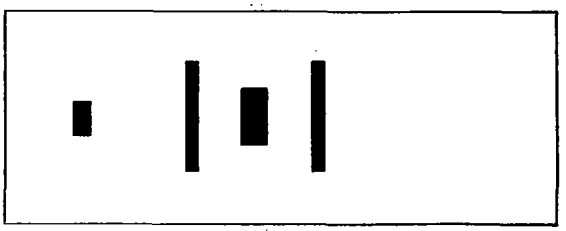
The fabrication process begins with a slice from a silicon crystal. The basic wafer or slice is a P-type material with a resistivity of 5-to-15 ohms-cm. The entire slice is covered with a layer of SiO_2. (Refer to Section II-B.) The first oxide removal (1st OR) mask is used and windows are chemically etched in the SiO_2 layer for the buried-layer diffusion; see Figure 1-11(a). The slice is placed in an oxidizing atmosphere with an N-type dopant. There, N^+ regions are diffused in the P substrate, directly under the future transistors' collector areas, to provide a very low resistivity material; see Figure 1-11(b). Next, the entire layer of SiO_2 is removed from the slice by etching with hydrofloric acid.

An N-type epitaxial layer is grown over the P substrate and N^+ regions by placing the slice in a high-temperature reactor, in the presence of hydrogen and silicon techrachloride with N-type impurities. After the epitaxial layer has been grown, a layer of SiO_2 is grown on the surface of the slice as before, providing a protective coating for the remaining manufacturing process steps; see Figure 1-11(c).

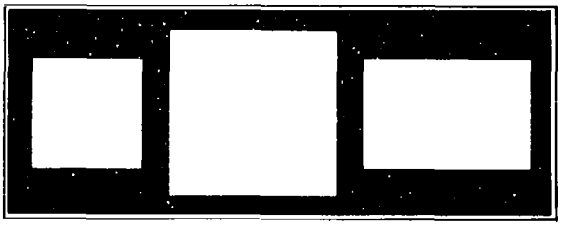
The remaining process steps are similar to the single and double-epitaxial process steps. Using the 2nd OR mask, areas are chemically etched through the SiO_2 for isolation diffusion; see Figure 1-11(d). Next, the slices are placed in a high-temperature furnace with an oxidizing atmosphere containing a P-type dopant. This isolation diffusion is the deepest and longest diffusion of the process, since it must penetrate the N-type epitaxial layer. A typical P-type isolation diffusion using boron requires a temperature of approximately 1200°C for about 20 hours. One of the advantages of the DUF process over the double-epitaxial process is that the isolation diffusion does not have to diffuse through the N^+ layer. As shown in Figure 1-11(e), the isolation diffusion forms isolated N-type areas which will be collectors for transistors and will also provide electrical isolation for the other components. As with the other diffusion steps, the oxygen atmosphere in the furnace re-oxidizes the cut-out areas of the slice surface and seals them against contamination. The silicon slice is again selectively masked using the 3rd OR mask, and is chemically etched to provide openings in the SiO_2 for the next diffusion; see Figure 1-11(f).



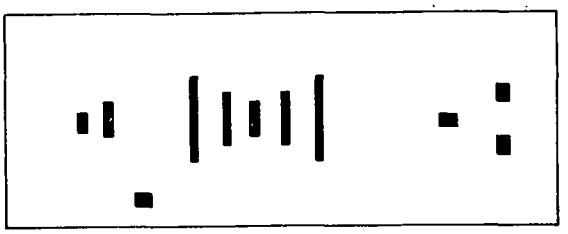
(A) FIRST O.R. MASK, BURIED LAYER



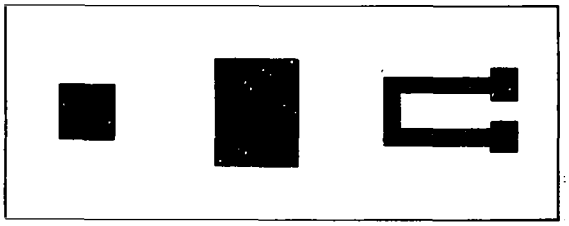
(D) FOURTH O.R. MASK, TRANSISTOR EMITTER, DIODE CATHODE, AND COLLECTOR CONTACT



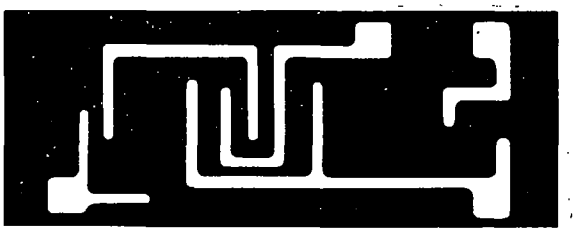
(B) SECOND O.R. MASK, ISOLATION



(E) FIFTH O.R. MASK, COMPONENT CONTACT



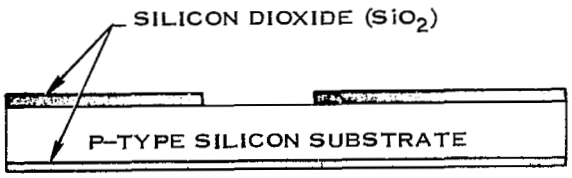
(C) THIRD O.R. MASK, TRANSISTOR BASE, DIODE ANODE, AND RESISTOR



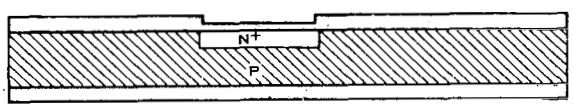
(F) METALLIZATION REMOVAL MASK

SC07031

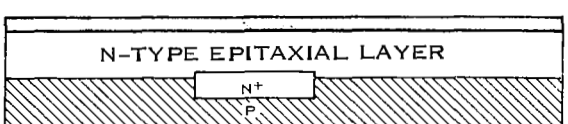
Figure 1-10. Set of Photographic Masks



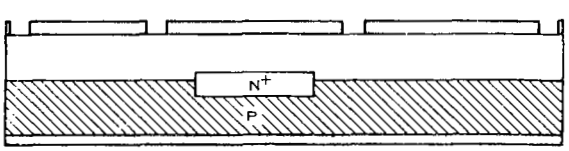
(A) FIRST OXIDE REMOVAL



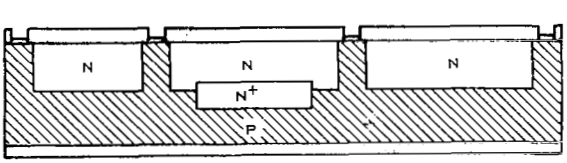
(B) BURIED N^+ REGION DIFFUSION



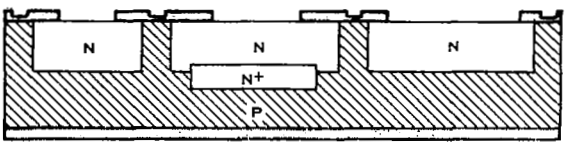
(C) SLICE, WITH EPITAXIAL LAYER GROWN FIRST, AND THEN OXIDE (SiO_2) LAYER GROWN OVER SLICE SURFACE



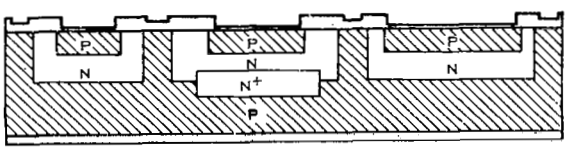
(D) SECOND OXIDE REMOVAL



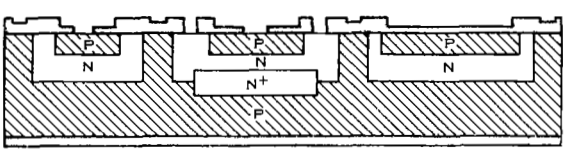
(E) ISOLATION DIFFUSION



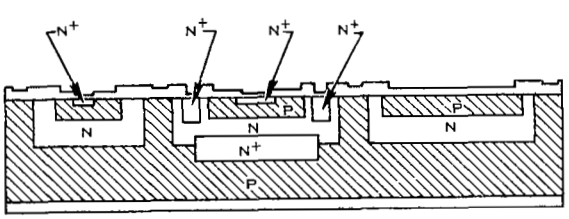
(F) THIRD OXIDE REMOVAL



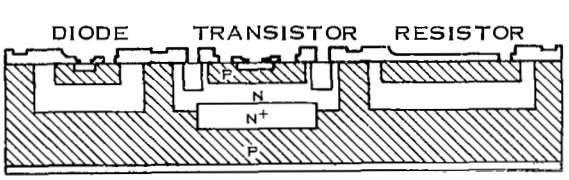
(G) TRANSISTOR BASE, RESISTOR, AND DIODE ANODE DIFFUSION



(H) FOURTH OXIDE REMOVAL



(I) DIFFUSION OF TRANSISTOR EMITTER, DIODE CATHODES, AND COLLECTOR CONTACTS



(J) FIFTH OXIDE REMOVAL

SC07032

Figure 1-11. Production Process Steps for Diffusion under Epitaxial Film

The next diffusion uses a boron source in a manner similar to that described for the isolation diffusion, except that the temperature is lower. During this diffusion step, the transistor's base, the diode's anode, and the resistors are fabricated; see Figure 1-11(g). The base diffusion requires much better process controls than the preceding diffusion, since the diffusion depth and surface concentration are important. To obtain better control, the base diffusion is always a two-step process. The process consists of predepositing the impurities into the open areas, and then these impurities are "driven-in" during the next step. The base-diffusion provides sheet resistivities of about 100 to 200 ohms/square. During the diffusion step, another layer of SiO_2 is simultaneously grown over the slice. The 4th OR mask is used to provide areas in the SiO_2 for the next diffusion; see Figure 1-11(h).

During the transistor-emitter diffusion, the diode cathodes and enhanced collector contacts are fabricated; see Figure 1-11(i). Also, when needed low-value diffused resistors are made for crossover points. These crossover points are used to intraconnect components in large circuits and arrays and are referred to as "tunnels." The diffused regions are heavily doped with N-type impurities to provide low resistivity (2 to 3 ohms/square). The diffusion depth for this step must also be held to a close tolerance. A typical emitter diffusion, using phosphorus, occurs at a temperature of between 1000°C and 1100°C.

After the emitter diffusion, a complete layer of SiO_2 is grown over the slice to provide sufficient oxide thickness for surface protection. This completes the manufacturing process of the individual components of the circuit. The components now must be intraconnected to provide the desired circuit. The last oxide removal, or 5th OR mask, is used to open contact areas in the SiO_2 for each component, and for the isolation or substrate; see Figure 1-11(j). The slice is then placed in a high vacuum chamber containing a metal evaporator. The evaporated metal is deposited evenly over the entire surface of the slice. Aluminum is most frequently used for the process; however, other metals have been and are being used, such as chromium, gold, silver, and nickel. The metal is selectively etched by a process similar to oxide etching, which leaves a pattern of intraconnections between the circuit components. The finished circuit, intraconnected, ready for mounting in a package and for connection to the package leads, is shown in Figure 1-12.

Up to this point in the manufacture of a monolithic microcircuit, only a small portion of the final cost of an individual circuit has been realized. The remaining manufacturing steps and the testing requirement represent a large portion of the total circuit cost. Because of this, extensive electrical testing is performed

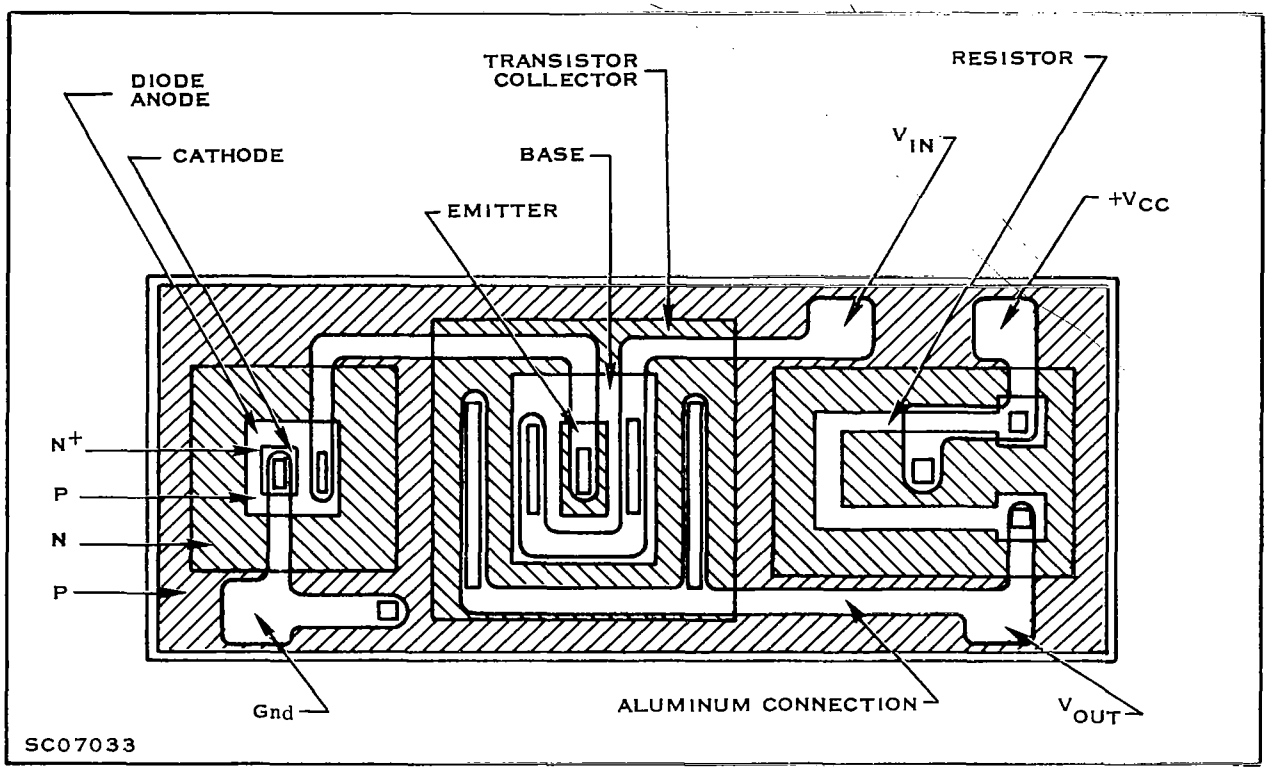


Figure 1-12. Finished Circuit

on the components, using an automatic multipoint probe. This automatic tester is computer controlled and performs several hundred electrical tests within a few minutes. Circuits not meeting the electrical tests are automatically marked and discarded.

The previous discussion has described the basic steps in the manufacture of monolithic microcircuits. There are many other necessary steps. Many process controls and quality assurance tests are performed during the process in order to provide a reliable circuit with the desired characteristics. Typical characteristics of each of the basic monolithic microcircuit structures are summarized in Table 1-1. The relative basic material cost is included for a comparison of the different processes; however, the material cost represents only a small part of the total device cost. The basic slice for the triple- and quad-diffused structures can be supplied by a semiconductor-material manufacturer more easily than the epitaxial structure.

Table 1-1. Structure Characteristics of Basic Types of Monolithic Microcircuits

Structure	Relative Cost of Material	Transistor R_{cs} (Ω)	Other Device Characteristics
Triple Diffused	X	<100	• PNP beta-to-substrate- >1.
Quad Diffused	X	< 100	• Isolated PNP and NPN transistors on single chip.
Single Epitaxial	5X	< 50	• Uniform collector concentration- lower R_{cs} than triple diffused. • PNP beta-to-substrate- >1.
Diffusion Under Epitaxial	10X	< 10	• High breakdown voltage. • PNP beta-to-substrate- << 1.
Double Epitaxial	10X	< 10	• Breakdown voltage less than diffusion under the epitaxial. • PNP beta-to-substrate- << 1.

D. COMPONENTS OF MONOLITHIC MICROCIRCUITS

1. General

The individual components of a monolithic microcircuit are somewhat different than discrete components. The components are connected together by back-biased isolation diodes. These diodes limit both the maximum voltage that can be applied to the components and the frequency response of the circuit. The active components, diodes and transistors are similar to discrete devices, except for the isolation diodes. However, the monolithic resistors and capacitors are quite different from their discrete counterparts. There are many variations of monolithic components used in industry, and the technology is changing and advancing monthly. A few of the monolithic components will be presented. The discussion will be based on their topological configurations and equivalent circuits.

2. Resistors

The monolithic resistor is a positive-temperature-coefficient semiconductor resistor. Monolithic resistors are made from silicon material, whereas, discrete resistors are made from materials such as carbon, metal film or wire. Monolithic resistors can be produced during either the base- or emitter-base-or emitter-diffusion process. Usually, resistors are fabricated during the base-diffusion step by diffusing a thin layer of P-type material into an isolated N-type region. The emitter-diffusion step is used to obtain a low-value resistor.

Since the resistor diffusion is the base diffusion of transistors, a somewhat limited compromise is made between the desired transistor characteristics and the necessary sheet resistivity. In some cases, it is necessary to adjust the process to obtain the desired transistor characteristics, and then afterwards to make another layout of the resistor topological pattern. Some manufacturers perform separate base and resistor diffusions. By doing this, it is possible to hold the transistor characteristics and to vary the resistor values to obtain a different resistor power transistor switching-time relationship. A typical P-type diffused resistor is illustrated in Figure 1-13.

The P-type, base-diffused resistors have sheet resistivities of about 100-to-200 ohms/square. The resistance is given in ohms/square ($\Omega/\square$), because this, typically, is the most useful way of specifying a given resistance. This measurement unit means that, measured between two opposite edges, a square of material will have a given resistance that is independent of the dimensions of the square.

The monolithic resistor model is a complex equivalent circuit, as shown in Figure 1-12. There is a significant capacitance to substrate, and a parasitic-distributed transistor from the resistor through the isolation region to the substrate. The parasite transistor produces a leakage current from the resistor to the substrate. At high frequencies, it becomes important to consider the distributed capacitance effect of the resistor. Resistors of relatively small cross section (0.5 mil) exhibit considerably less capacitance than wider resistors of equivalent value. This capacitance varies from 0.75 pF for a 0.5-mil resistor to 3.0 pF for a 1-mil resistor of the same value.

The diffused resistors usually do not have precision values. Their absolute values vary, typically, by 20 percent, and they may vary as much as 50 percent, although resistance ratios on any single bar are usually within 2 percent. The temperature coefficient is typically 1200-to-1600 parts-per-million-per-degree centigrade, but the resistance ratio of 2 percent will be maintained over a temperature range of 100°C. The temperature coefficient is a function of sheet resistance, as shown in Figure 1-13.

3. Capacitors

The capacitors used for monolithic microcircuits differ considerably from their equivalent counterparts in discrete components. Two basic types of capacitors are used in monolithic microcircuits. One type is a back-biased PN junction which

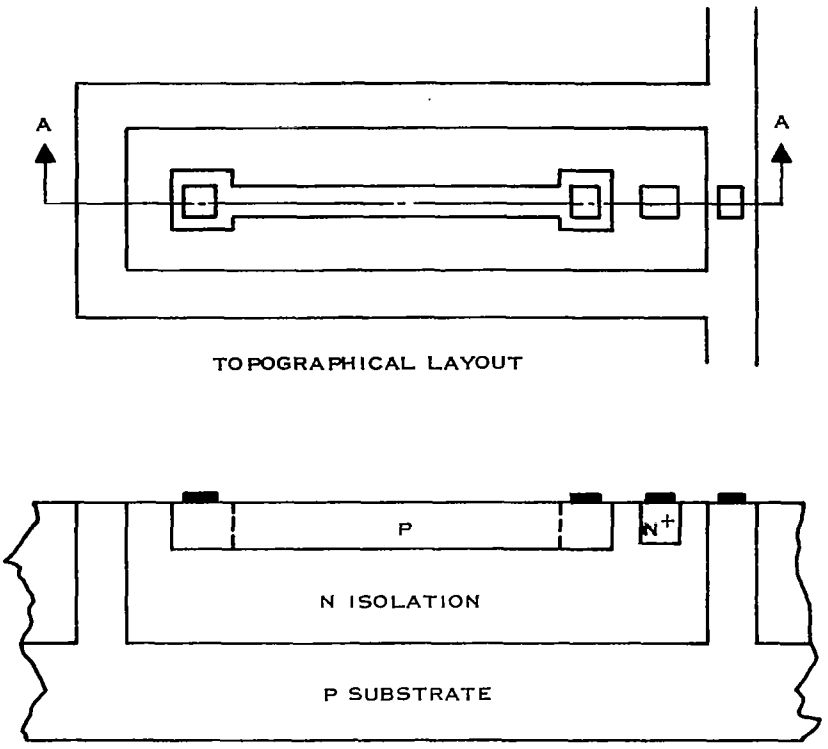


Figure 1-13. A Typical Monolithic P-Type Diffused Resistor and Its Principal Characteristics (Sheet 1 of 2)

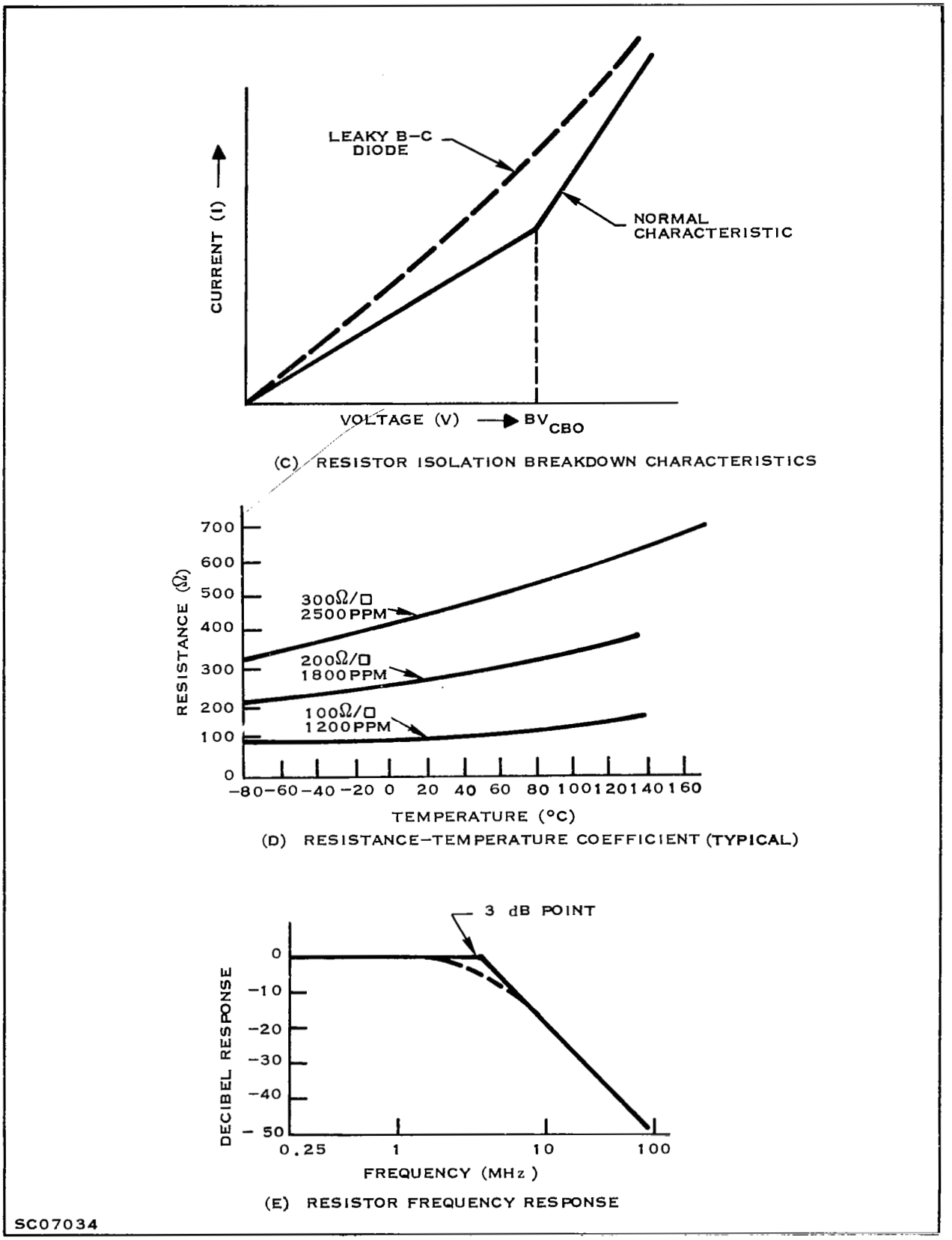


Figure 1-13. A Typical Monolithic P-Type Diffused Resistor and Its Principal Characteristics (Sheet 2 of 2)

provides a high capacity per unit area and requires no additional process steps. The other type is a metal-oxide-semiconductor (MOS) capacitor; its characteristics are closer to those of the discrete capacitor.

The simplest method for manufacturing diffused capacitors is to use the base-collector diffusion to obtain a PN junction (Figure 1-14). This type of capacitor is polarized, and the depletion region actually serves as the dielectric between the two plates. The width of the depletion region is a function of the reverse bias across the junction, thus forming a voltage-sentive capacitor. With zero bias applied, the depletion region is extremely narrow and creates a relatively high capacitance.

The equivalent circuit for the PN junction capacitor is shown in Figure 1-14. Its limitations consist of a series resistor and a shunt parasitic capacitor (C_1). The ratio between C and C_1 ranges between 5-to-1 and 2-to-1. The available capacity is about 0.2-to-0.6 pF/square mil. The capacity can be increased to about 1 pF/square mil by using the emitter diffusion step. This type of PN junction capacitor is shown in Figure 1-15, and its equivalent circuit is similar to the one shown in Figure 1-14.

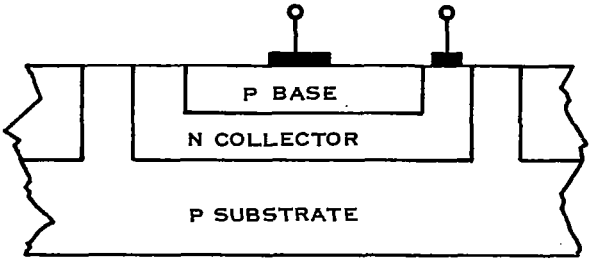
This capacitor is composed of a single P-type plate, which is the base diffusion, and two outside plates, which consist of the N-collector region for the lower plate and the N-emitter region for the upper plate. The two outside plates are electrically shorted together during the diffusion process, thus providing two parallel, back-biased junctions with about twice the capacitance of one junction. The collector-base capacitor has a relatively high breakdown voltage (about 50 V), whereas, the other PN junction capacitor has a breakdown of about 9 V.

The other type of capacitor used in monolithic microcircuits, the MOS capacitor, uses the silicon dioxide as the dielectric. The two plates consist of the low-resistivity, emitter-diffusion region and the intraconnection-metalization (usually aluminum). The cross section view and equivalent circuit for the MOS capacitor is shown in Figure 1-16.

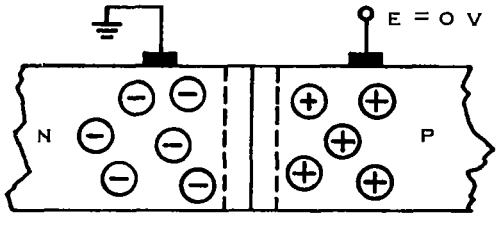
The MOS is a nonpolar device and is not voltage sensitive. It has a maximum working voltage of approximately 20 V and a capacity of about 0.3 pF/square mil of metalized area. It has less shunt capacitance to substrate than the PN junction capacitor. The MOS capacitor usually requires an extra process step to control the dielectric thickness, and for a given capacitance requires more die area.

4. Transistors

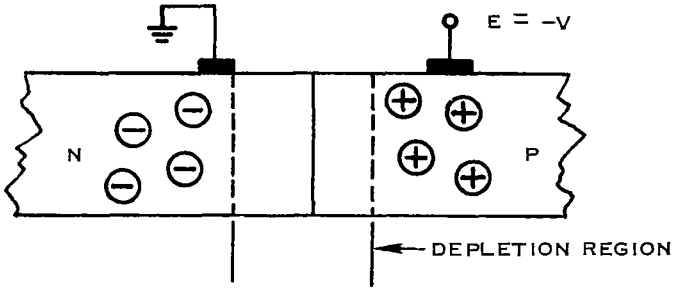
Many types of monolithic transistors are available. Several layouts of monolithic transistors are shown in Figure 1-17. This is partially the result of the variety of circuit-function requirements and the variations in topographical layout



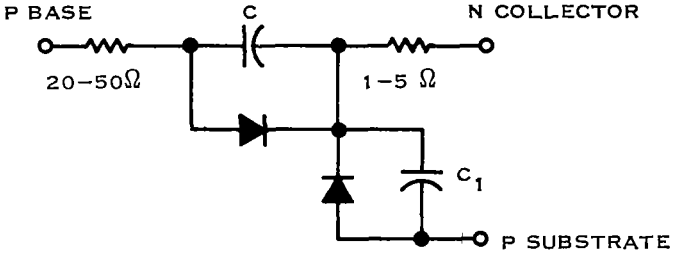
(A) CROSS SECTION VIEW



(B) ZERO BIAS



(C) REVERSE BIAS



(D) EQUIVALENT CIRCUIT

SC07035

Figure 1-14. P-N Diffused Junction Capacitor

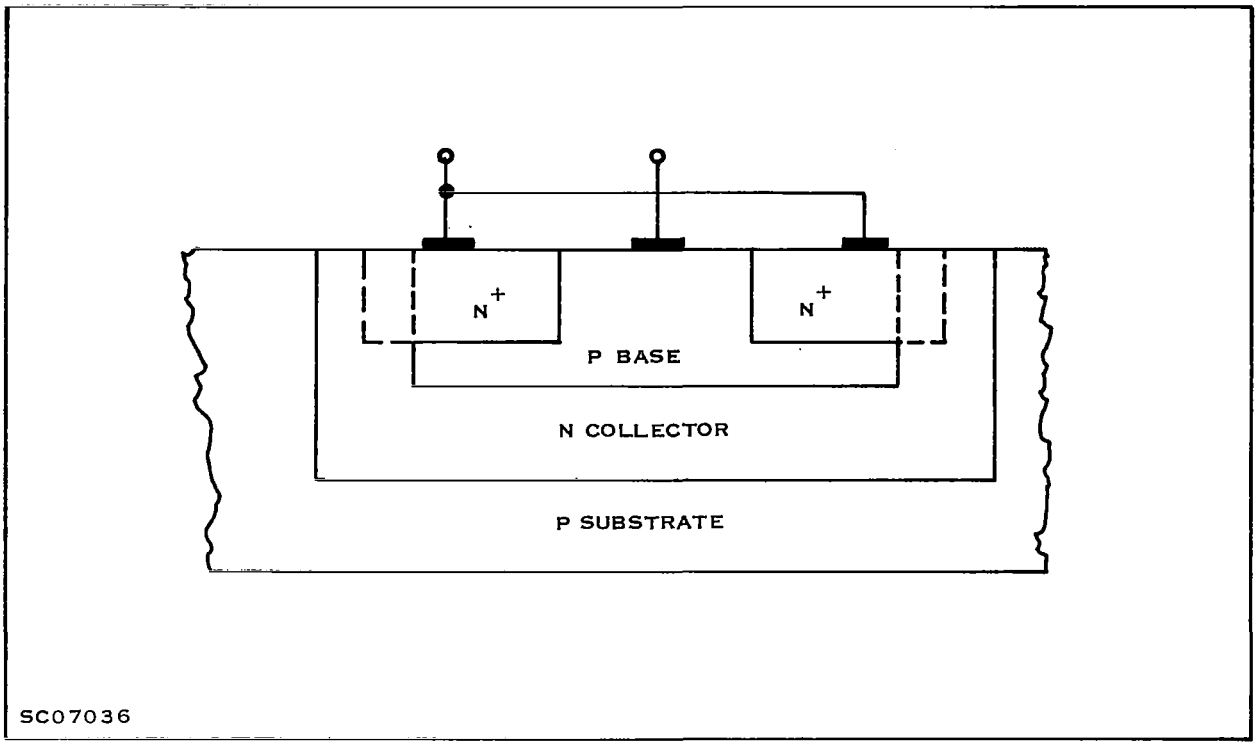


Figure 1-15. P-N Junction Capacitor

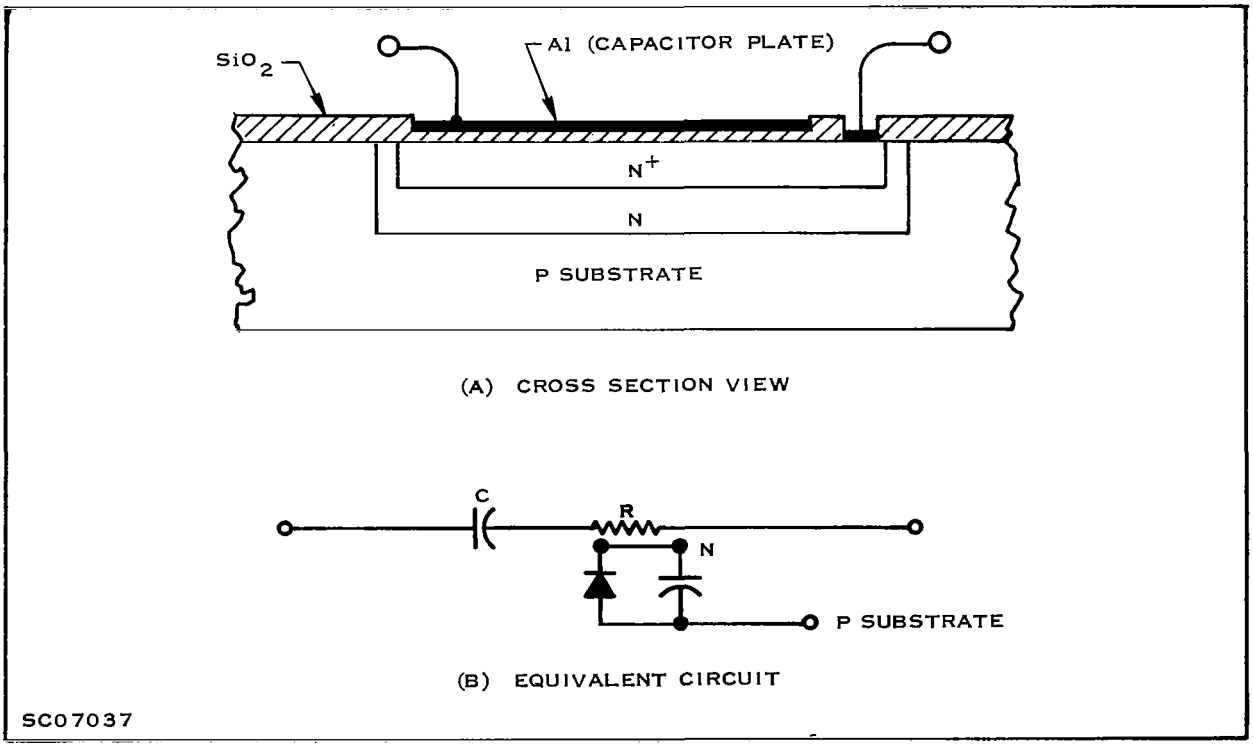


Figure 1-16. MOS Capacitor

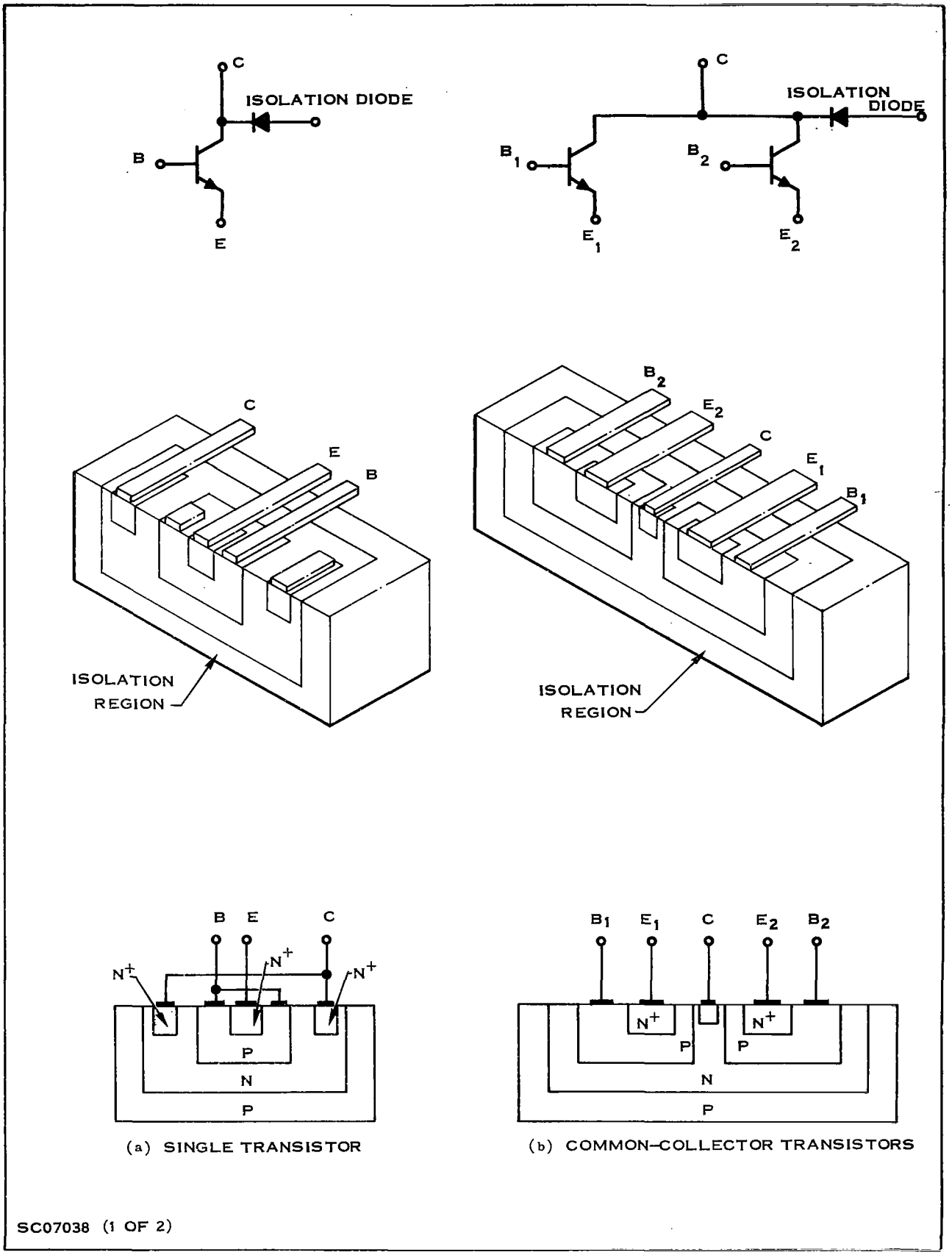


Figure 1-17. Typical Layouts for Monolithic Transistors (Sheet 1 of 2)

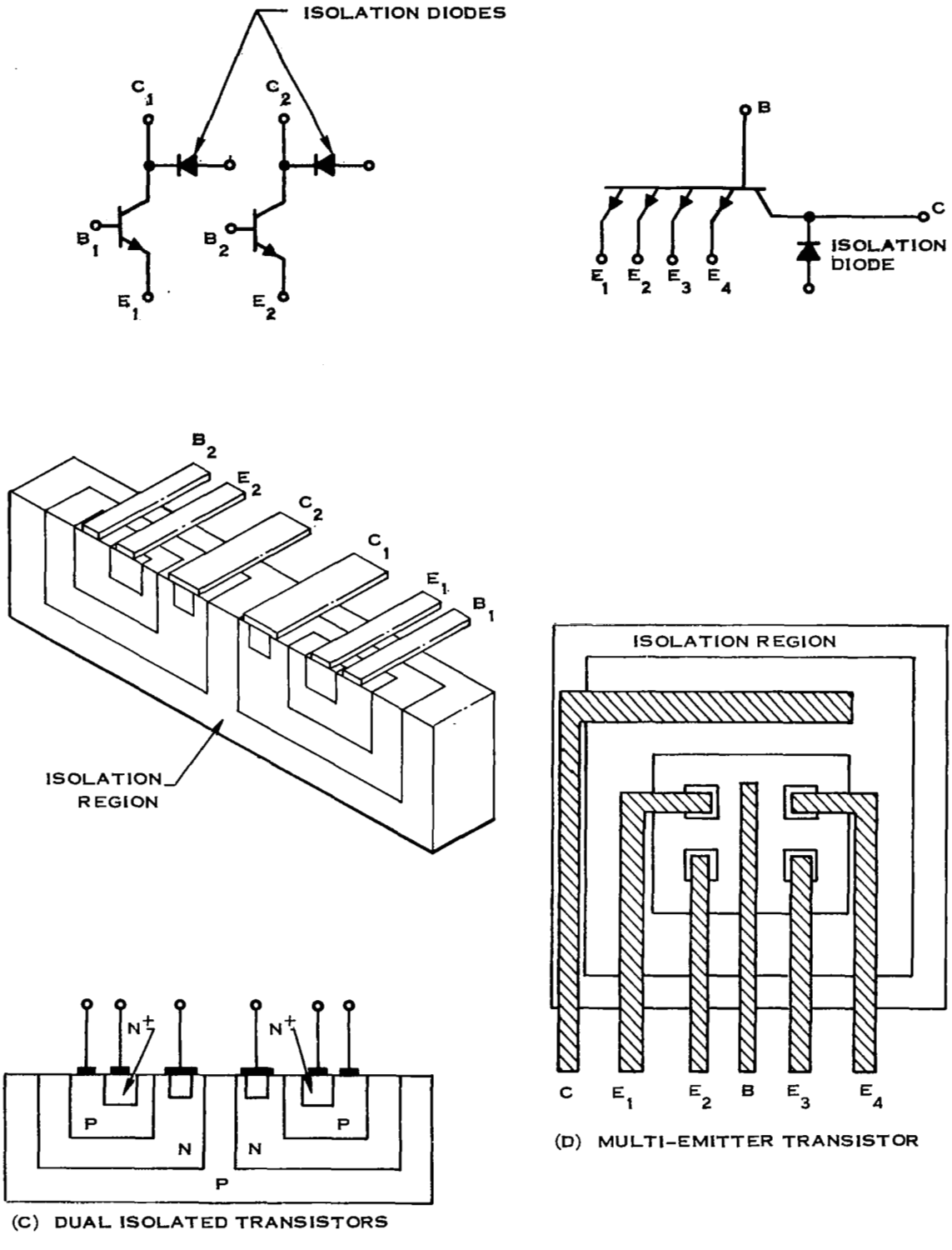


Figure 1-17. Typical Layouts for Monolithic Transistors (Sheet 2 of 2)

and process design. Monolithic transistors are no more expensive to fabricate than other components, and in some cases are less expensive; they offer a better circuit function, lower power dissipation, and better drive capabilities. As an example of the advantage of using monolithic transistors instead of capacitors, a monolithic flip-flop may contain as many as 30 transistors, offering a functional capability not obtainable from a design based on discrete components. The superior functional capability is gained from the inherent matching of transistor characteristics which occurs between monolithic transistors on the same die. As with monolithic resistors, transistor characteristics are matched within five percent maximum,and they will hold this tolerance across the specified temperature range.

Monolithic transistors have some disadvantages, but new concepts have minimized these to a useable level. For instance, the parasitic capacitance of the collector, due to the collector-to-substrate PN junction, limits the frequency response of the circuit. New isolation techniques and smaller geometry are providing circuits with frequency response greater than 100 MHz. Another disadvantage is the high collector-saturation resistance. A monolithic transistor has a saturation resistance of 10 to 100 Ω, compared to 5 to 20 Ω for discrete transistors.

The majority of monolithic transistors are NPN type, but in some circuits (linear for example) it is desirable to have PNP transistors. In triple-diffused and epitaxial structures, a PNP transistor can be obtained by using the substrate as a collector; however, this limits its use, since the substrate is connected to the lowest potential. This type of PNP transistor can only be used in an emitter-follower application. The quad-diffused structure provides an isolated PNP transistor and is used for several linear circuits. In both cases, the resultant PNP transistors have low betas. A typical equivalent circuit for a monolithic transistor is shown in Figure 1-18.

5. Diodes

It is most economical to form diodes , as well as other components, during the diffusion steps used to form transistors. Therefore, diodes are fabricated by using either the base-to-collector or the base-to-emitter PN junction.

A diode formed by the base-to-collector junction has a high-breakdown voltage (approximately 50 V) and a storage time as high as tenths of microseconds. This type of diode is illustrated in Figure 1-19(a). The emitter can be shorted to the base or not diffused-in during the process.

The base-to-emitter diode has a relatively low-breakdown voltage (5 to 6 V but provides a high-speed, low-conductance diode. The base-to-emitter diode is illustrated in Figure 1-19(b), with the collector area unconnected.

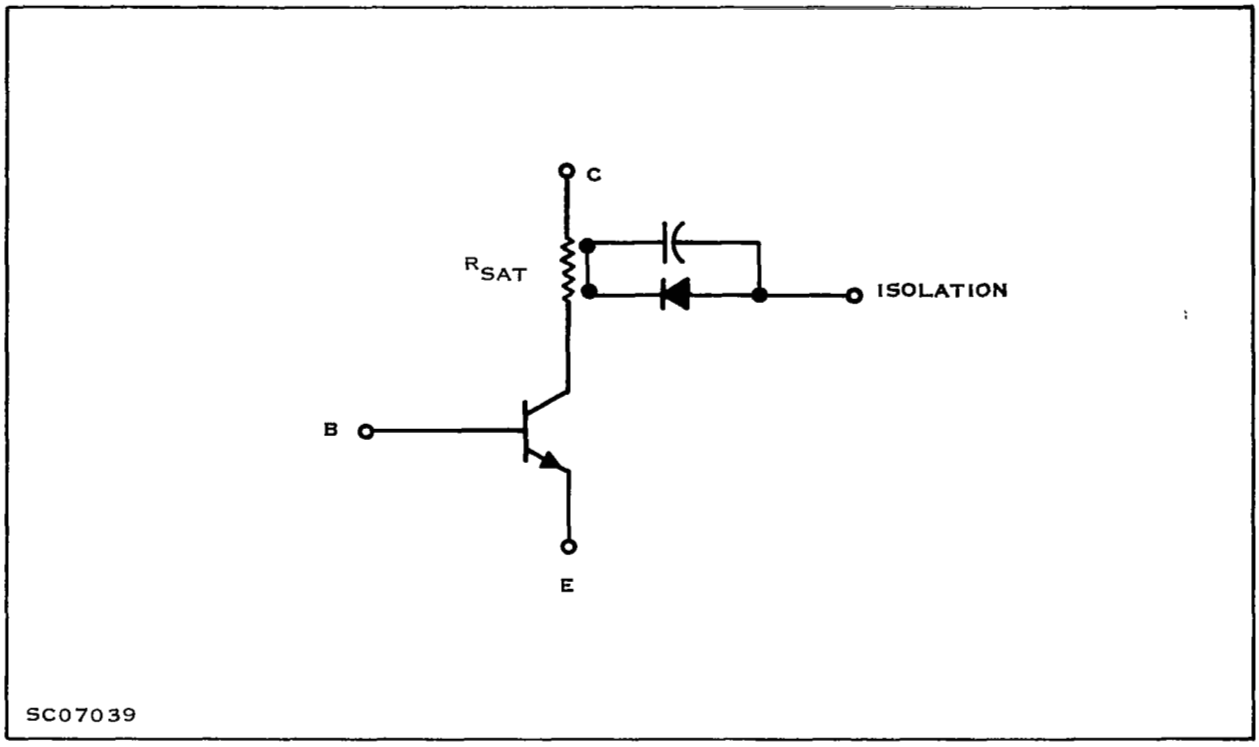


Figure 1-18. Typical Equivalent Circuit of A Monolithic Transistor

The conductance of any monolithic diode is less than that normally associated with a conventional diode, because of the higher bulk-resistance associated with the upper contact of the collector or because of the nonoptimum diffusion schedules that are used to form the diodes.

A multiple diode array, commonly used to provide DTL gate inputs, is shown in Figure 1-20. The collector and emitter are shorted together during the diffusion process. The diodes' anodes are shorted together with the metallization. The multi-emitter transistor can be used as a diode array by shorting the base to the collector.

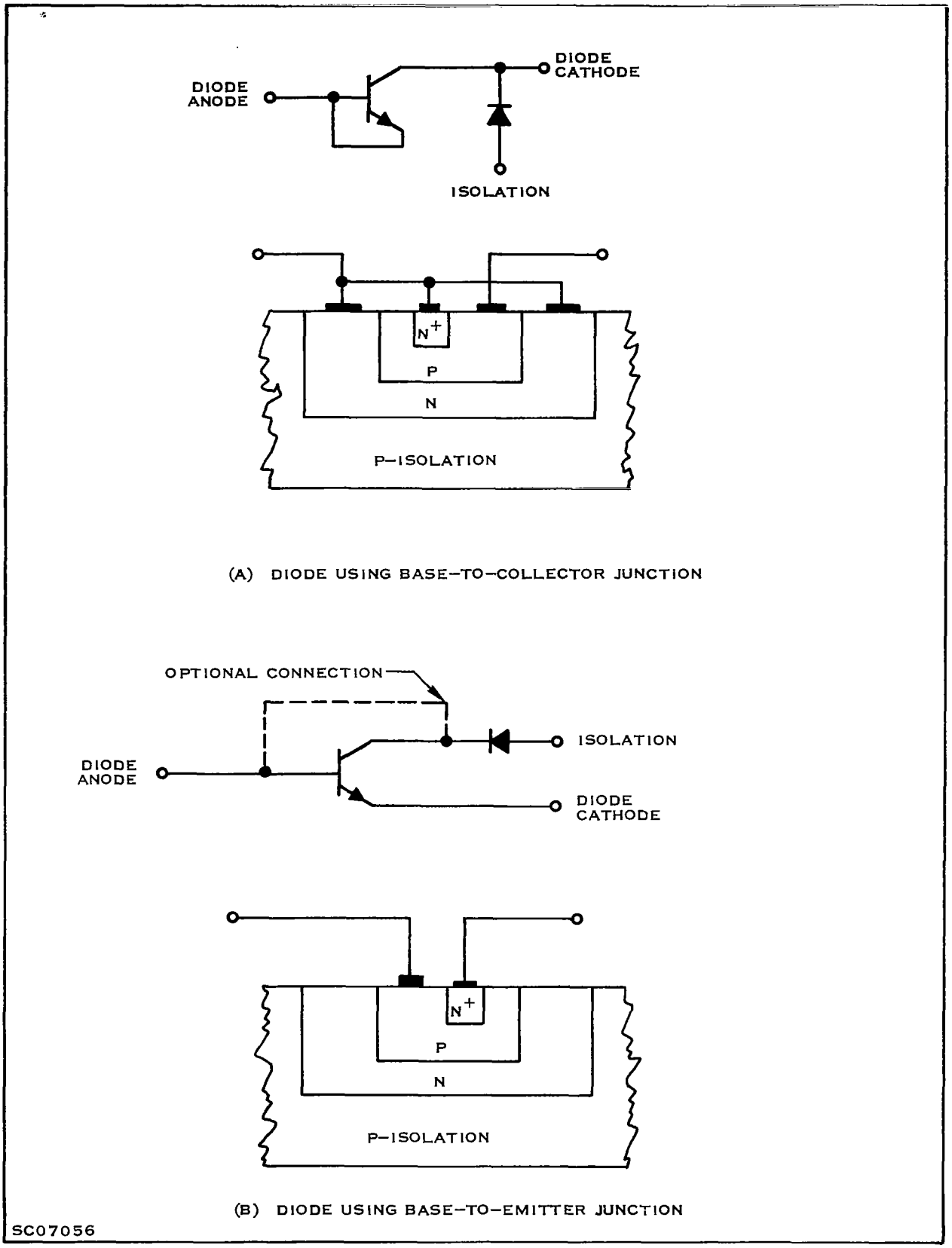


Figure 1-19. Monolithic Diodes

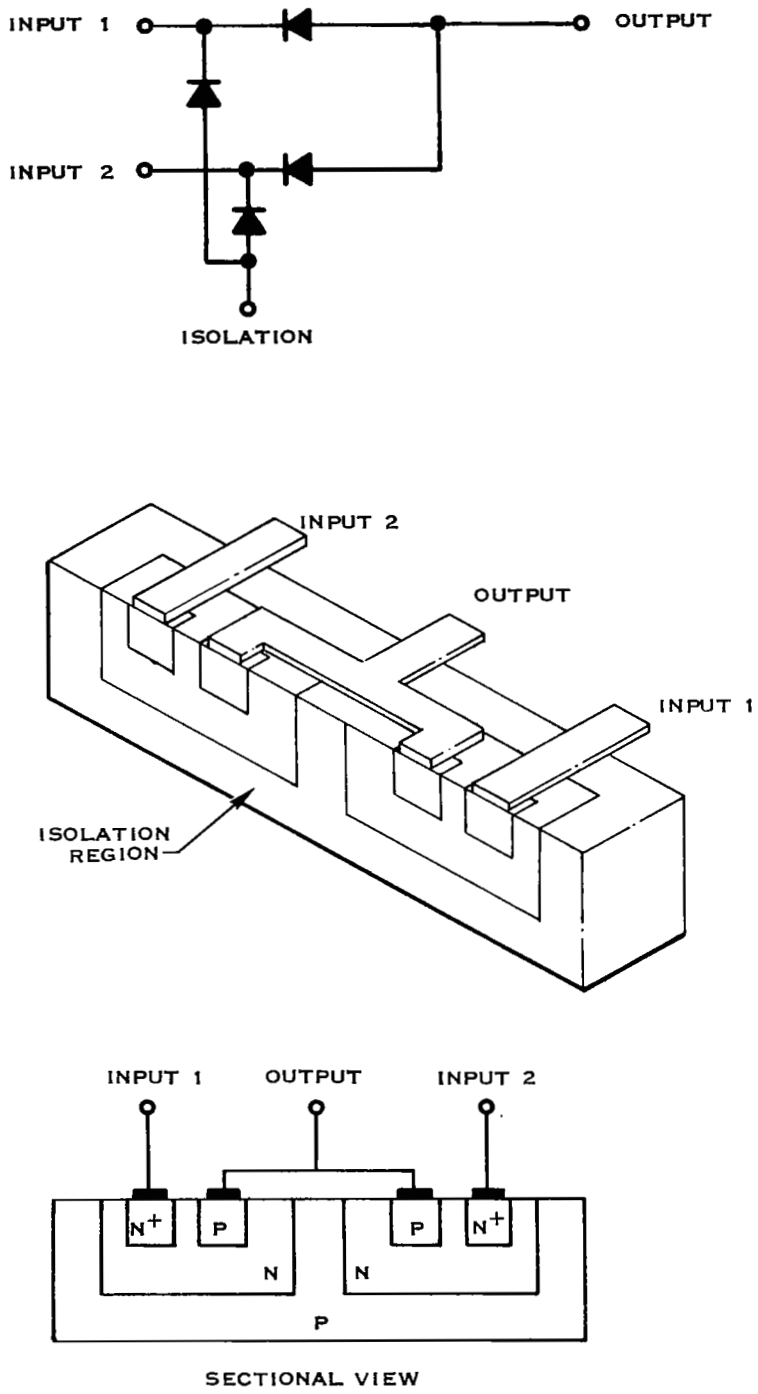


Figure 1-20. Input Diode Array

SECTION III

DIGITAL MONOLITHIC MICROCIRCUITS

A. LOGIC CIRCUIT FAMILIES

1. General

The basic logic functions can be performed with different combinations of the OR, AND, and NOT circuits shown in Figure 1-21. System design with these circuits is tedious, since each level must be uniquely designed. To employ a standard design approach (imperative for monolithic microcircuits) each gate must be followed by an inverter, in which case, the circuits become NAND or NOR gates.

Many logic families have evolved that utilize different combinations of active and passive components to implement the logic function. The early monolithic microcircuits followed closely the familiar discrete-component schemes. Component count was kept low in early circuits, and the use of transistors was minimized due to their relative expense. As monolithic microcircuit technology advanced, it was found that transistors were less expensive to fabricate than other elements, and the latest circuits follow this scheme.

Only the most common types of logic families used for monolithic microcircuits will be discussed here. These families range from a "component-by-component replacement of a discrete-component" scheme, through several modified schemes, to the "transistors are cheap" philosophy, and the multiple-emitter transistor. These examples are typical representatives of the basic families, and by no means cover all the variations of existing monolithic microcircuits. The monolithic microcircuit families that will be discussed are:

1) Direct-coupled Transistor logic (DCTL)

2) Resistor-transistor logic (RTL)

3) Resistor-capacitor-transistor logic (RCTL)

4) Diode-transistor logic (DTL)

5) Transistor-transistor logic (TTL)

6) Emitter-coupled logic (ECL)

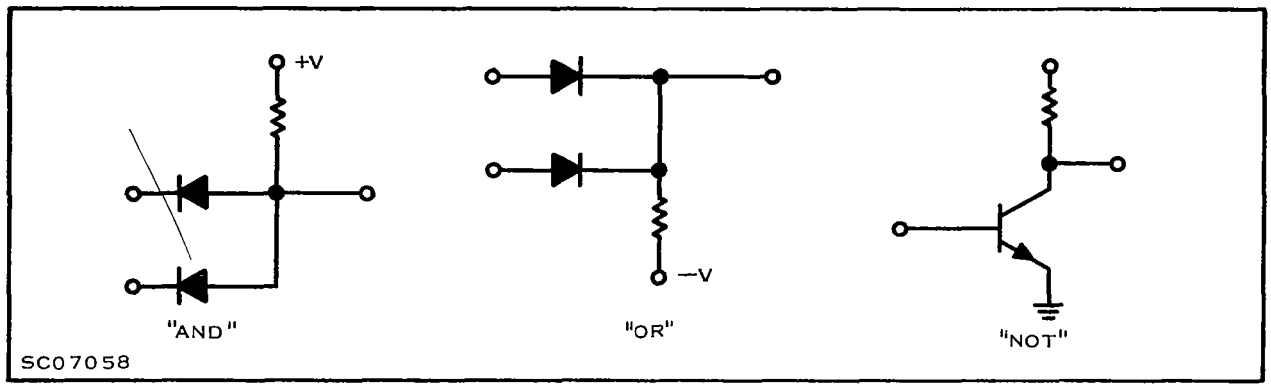


Figure 1-21. Basic Logic Circuits

2. Direct-Coupled Transistor Logic (DCTL)

Direct-coupled transistor logic (DCTL) was one of the first practical monolithic logic circuits. The basic circuit is shown in Figure 1-22. The DCTL circuit is ideal for monolithic processing, since it contains multiple transistors in a common isolation region. By making the collector load resistance small, it can provide a relatively high switching speed. The principal shortcoming of DCTL is input base-current-hogging. This condition is a result of a very minor V_{BE} mismatch between gates fanning out from a common output node. The input with the lowest threshold will absorb excessive current, leaving insufficient drive for the other inputs. Current-hogging limits the fan-out and speed performance of DCTL, and therefore, this logic circuit has very limited use in system application.

3. Resistor-Transistor Logic (RTL)

The basic resistor-transistor logic (RTL) gate configuration is shown in Figure 1-23. The configuration is the same as that of the DCTL circuit, except for the addition of an input resistor, R_2. The addition of R_2 forces some of the input voltage to appear across R_2, and the base currents are more evenly divided between parallel inputs. By increasing R_2, high fan-out is achieved with no current-hogging; however, as R_2 is increased, the switching speed of the circuit is reduced. A design compromise must be made between high fan-out and high switching speed when using an RTL circuit.

4. Resistor-Capacitor-Transistor Logic (RCTL)

The current-hogging shortcoming of the DCTL circuit family was minimized in the RTL circuit. The switching speed for the RTL circuit can be increased by shunting the input resistor with a capacitor. This is the resistor-capacitor-transistor logic (RCTL) configuration, as shown in Figure 1-24.

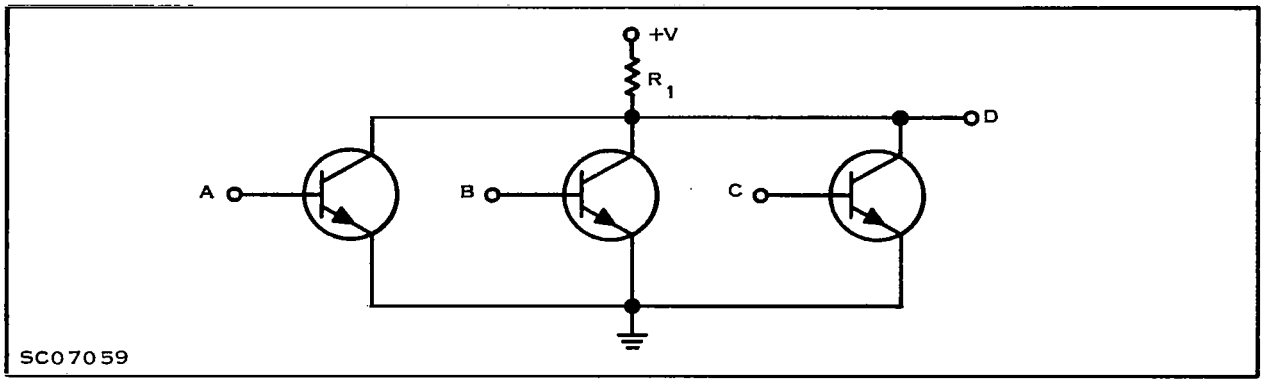


Figure 1-22. DCTL Gate

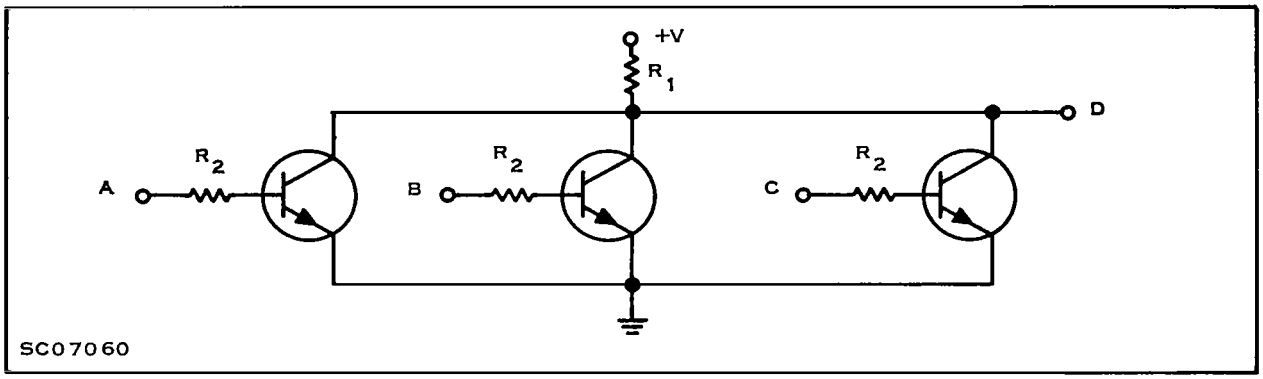


Figure 1-23. RTL Gate

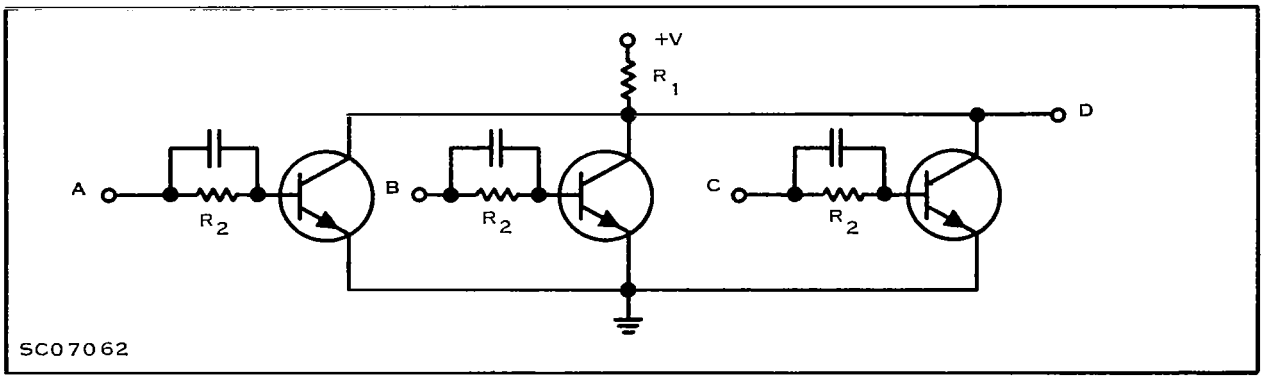


Figure 1-24. RCTL Gate

The value of R_2 ranges from approximately 450 Ω in the RTL circuit to 20 kΩ for the RCTL series. Increasing the value of R_2 not only increases the fan-out capabilities but also provides a low-power circuit. While the addition of R_2 increases the required static voltage swing, the bypass capacitor, C, dynamically clamps the output collector to the base of the input stage. Thus, only a small portion of the static swing is required to dynamically switch the load. The RC coupling network in the RCTL structure permits the circuit to operate at a low-current standby level, but allows the generation of high dynamic currents from small voltage swings that occur during switching.

As a consequence, RCTL is more sensitive to turn-on noise than RTL, and is about as sensitive as DCTL. If the limiting static-base current is the same in DCTL, RTL, and RCTL designs, the turn-off noise immunity will be the same for DCTL and RCTL and somewhat better for RTL, all other factors being equal. Due to the high-pass characteristic of the RC network, RCTL will have superior noise performance in a low-frequency noise application.

Although RCTL has been used in many low-power, medium-speed applications, the circuit has one disadvantage for monolithic construction—the fabrication of capacitors on the same substrate as resistors and transistors.

5. Diode-Transistor Logic (DTL)

The basic diode-transistor-logic (DTL) configuration is shown in Figure 1-25(a). Here again, a discrete-component philosophy was used. The DTL circuit was a familiar logic scheme for discrete component design; therefore, it has proven popular in retrofitting with microcircuits those systems that have discrete-component DTL. The advantages of the basic DTL circuit are that it has a relatively good power-speed trade-off and good dc noise margin. There are two disadvantages to the basic DTL circuit, the first one being the close-tolerance resistors that are required, for this requirement reduces the fabrication-process yield and increases the customer cost. The second disadvantage is that to achieve high switching speeds, either the coupling and input diodes must have different characteristics (hard to achieve in monolithic form) or a separate power supply (a definite disadvantage) must be used to turn off transistor Q_1 of the equivalent circuit. To eliminate some of the problems that existed in the basic DTL monolithic microcircuits, several variations were attempted. Most of them took advantage of the "transistors are cheap" philosophy of monolithic construction.

One modified DTL circuit, shown in Figure 1-25(b), was developed by substituting an intermediate transistor-gain stage for one of the offset diodes. The addition of the emitter-follower stage (Q_1) offers several advantages over the basic DTL circuit:

- It eliminates the necessity of producing low-speed, high-stored-charge diodes in the same monolithic bar with fast input diodes.
- It eliminates the necessity of a negative power supply.
- It provides faster switching times. The collector of Q_1 is connected to a tapped resistor (R_1 and R_2) which prevents the transistor from ever going into saturation. The emitter-follower provides additional drive current to the output transistor, Q_2, without requiring high-input currents when the input is in the low state. The additional drive to the output transistor invites the use of a smaller base resistor, R_3, and relaxes the beta requirement of the output transistors.

From a dc standpoint, the output collector-resistor, R_4, is necessary only to provide input-diode leakage current plus noise protection; therefore, R_4 should be as large as possible to minimize collector saturation current. However, to achieve better switching times, R_4 should be low enough to supply the necessary charging current for the output loading capacitance, which consists of the circuit output capacitance, system wiring capacitance, and the input gate capacitance multiplied by the fan-out. This capacitance driving problem poses the usual design compromises between power and fan-out or speed.

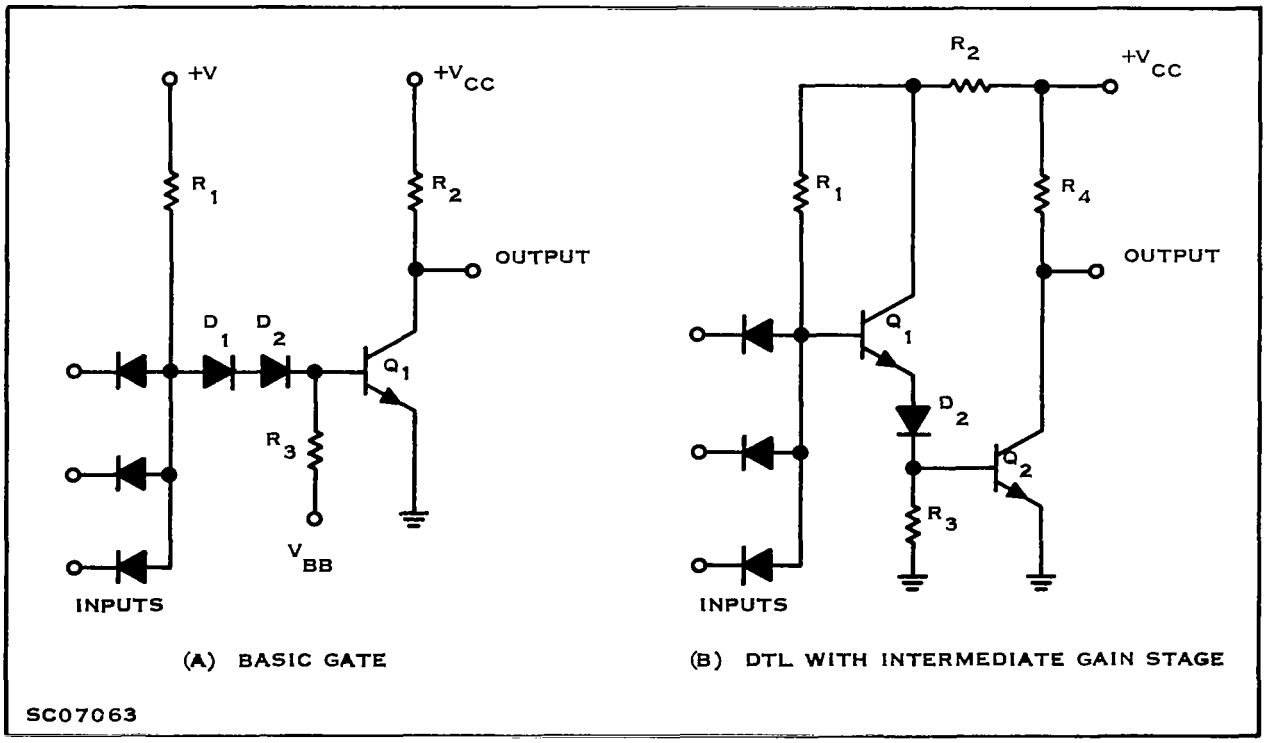


Figure 1-25. DTL Gate Circuits

6. Transistor-Transistor Logic (TTL)

The transistor-transistor logic (TTL) circuit, shown in Figure 1-26(a), is analogous to the DTL circuit in certain respects. When TTL was developed, it made use of the economical feasibility of using transistors instead of diodes, and also solved the capacitive loading problem. The input transistor offers a significant advantage in switching time over the diode input of DTL. The addition of the phase-splitter driver and push-pull buffered-output circuit provides good noise rejection and excellent drive characteristics into capacitive loads.

As shown in Figure 1-26(b), a low voltage at inputs A or B will allow current to flow through the diode associated with the low input, and no drive current will pass through diode D_3. When inputs A and B are raised to a high voltage, the drive current will then pass through diode D_3.

As shown in Figure 1-26(c), the multiple-emitter transistor of the TTL circuit performs the same function as the diodes in the DTL circuit. However, the transistor action of the multiple-emitter transistor causes transistor Q_1 to turn off more rapidly, thus providing an inherent switching-time advantage over the DTL circuit.

When the inputs of the TTL circuit are high, there is an inverse transistor action between the emitter and the collector of the input transistor. If each emitter is connected to a different driving source at slightly different potentials, leakage currents mount up and detract from base-drive to other similar gates. This is similar to the current-hogging problem associated with DCTL circuits. Unlike current hogging in DCTL, the TTL structure process offers an independent control of the effect. By using special geometry techniques and optimized diffusion schedules, the inverse beta can be held to a value that is less than one; thus, the input leakage current is reduced to an acceptable value. In comparison, the maximum input leakage current of the TTL is approximately 40 μA, whereas it is 5 μA for the DTL.

Although the multiple-emitter transistor is not a familiar discrete component, it is really an economically feasible component in monolithic circuits. A common collector tank is diffused, a common base is diffused in the collector, and then emitters are diffused into the one base. One advantage is that more circuitry per area can be obtained; hence, there will be more circuitry per chip. Also, the smaller geometry leads to a second technical advantage—a faster speed that results from lower capacitance associated with the smaller area.

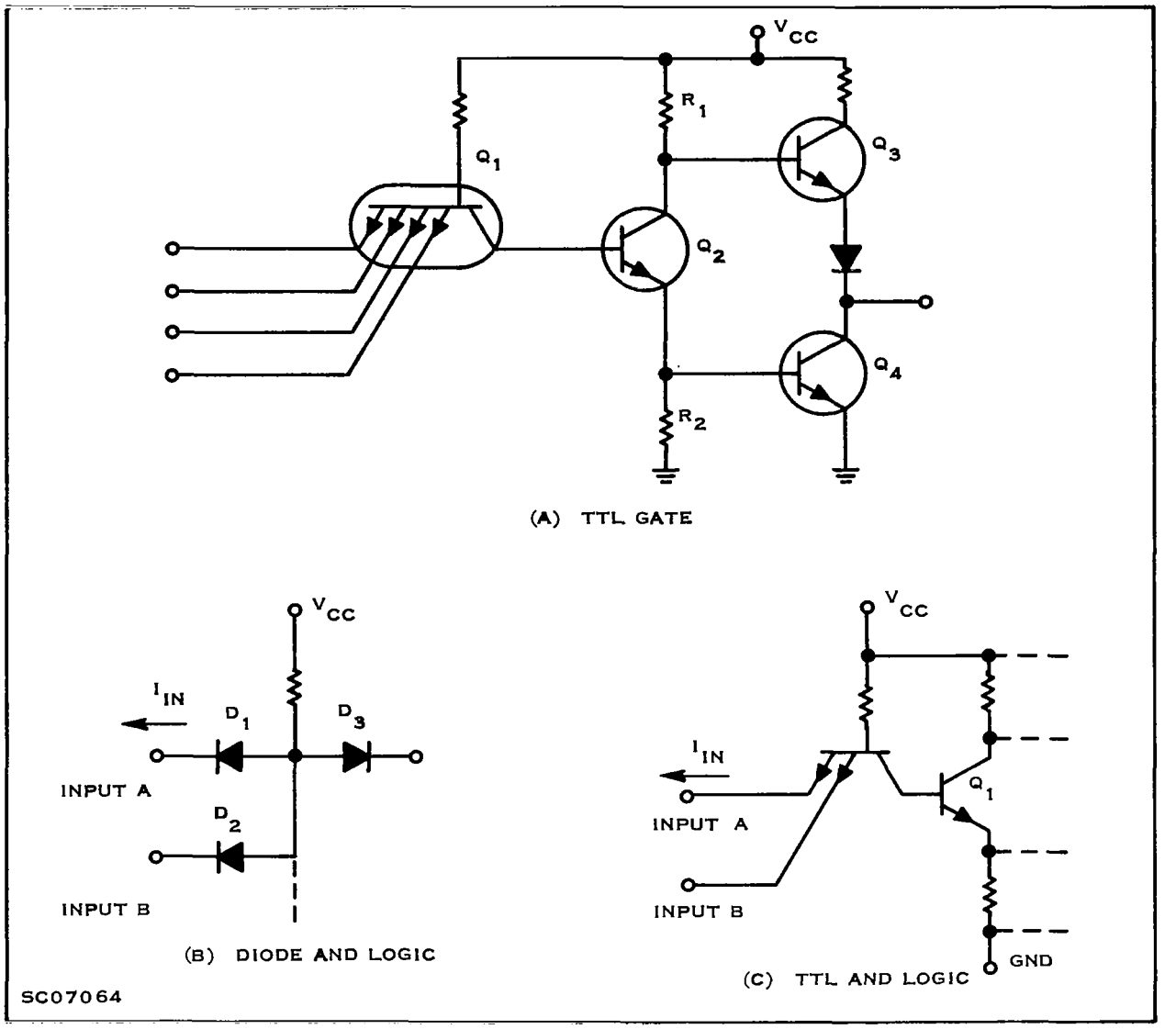


Figure 1-26. TTL Circuits

Referring to Figure 1-26(a), the TTL configuration employs a circuit which has a very low output impedance for high-capacity drive capability, high fan-out and good noise immunity. When the inputs of the circuit are high, Q_2 and Q_4 are driven "on" as grounded emitter amplifiers. Transistor Q_3 and its emitter diode are both slightly forward-biased but conduct only a negligible amount of current. When one of the inputs is low, Q_2 and Q_4 are both cut off, and Q_3 conducts as an emitter-follower. The output is, therefore, pushed and pulled up and down by a transistor turning "on."

As with other logic configurations, several power-speed compromises were made. The particular value of R_1 was chosen to give the lowest possible power dissipation, whereas, R_2 was selected to give excellent turn-off switching-time

characteristics on the output transistor, Q_3. The multiple-emitter transistor, Q_1, is used to pull stored charge from the base of Q_2 when the input voltage is lowered.

7. Emitter-Coupled Logic (ECL)

A form of unsaturated logic which is effective for very high speed applications is emitter-coupled logic (ECL), shown in Figure 1-27. Thus, the switching tim of transistors can be greatly reduced if they are operated in the active region and are prevented from going into saturation. The typical ECL circuit is designed with a differential input amplifier, with parallel-transistor gating on one side. The voltage reference input (V_{REF}) on the opposite side defines the logic threshold level for the circuit. The differential input circuit is followed by emitter-followers which provide complementary outputs.

When inputs A and B are below the reference voltage, output C is at the "low" logic level, and $\overline{C}$ is at the "high" logic level. When either A or B is changed to a voltage above V_{REF}, output C will also change to a "high" logic level and $\overline{C}$ will change to a "low" logic level. High speed is obtained by keeping the transistors out of saturation with a restricted signal swing, while noise immunity depends upon output voltage range and the symmetry of "1" and "0" levels with respect to the reference voltage.

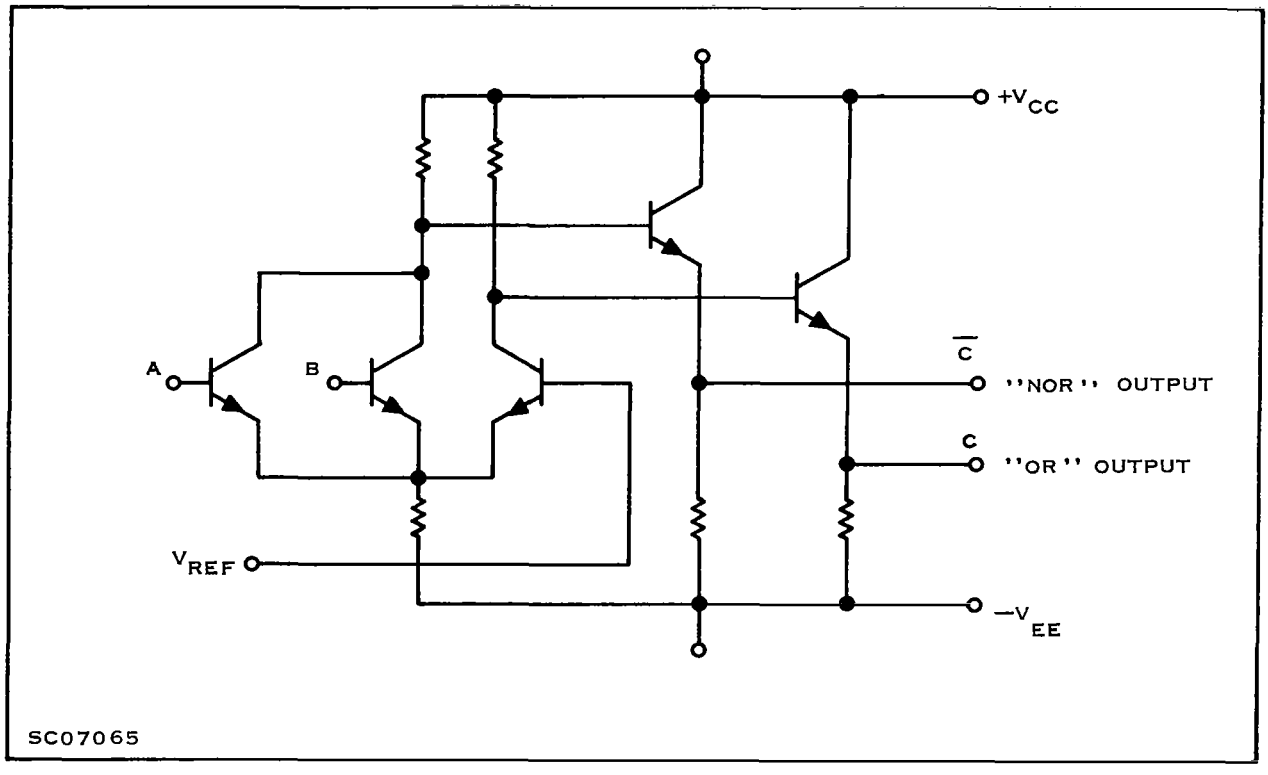


Figure 1-27. ECL Gate

The emitter-followers' outputs are used to provide high fan-out to restore the dc levels and to drive terminated or constant-impedance matched lines—a definite requirement for a circuit operating with propagation rates in the 2 ns range.

Monolithic circuits of the ECL type, with propagation delays in the 1-to-2 ns range, have been demonstrated, and circuits with maximum propagation delays of 5 to 10 ns are available. Actual design of ECL circuitry is complex in comparison to the design of saturating circuits,due to the many dependent variables which must be considered. As with other families, when the switching speed is decreased, the power requirement is increased. The range of the electrical parameters for the different families will be presented later in this discussion.

B. DEFINITIONS OF DIGITAL CIRCUIT PARAMETERS

1. General

There are several parameters that should be understood before selecting a monolithic microcircuit. When using microcircuitry, the design engineer is actually working with a group of subsystems, and he will be using somewhat different parameters than if he were designing with discrete components. The material presented here defines the parameters used to characterize digital microcircuits but does not include the fundamentals of logic design.

At this time there is very little standardization in microcircuit characteristics, parameters, and symbols. A registration format for semiconductor microcircuit logic-gating circuits, prepared by Electronic Industries Association (EIA) committees, is now available. It is the first attempt to standardize on monolithic microcircuit specifications. The committee members found it impossible to arrive at a universal specification for all logic families. Therefore, they specified the necessary parameters for microcircuit data sheets and presented recommended testing conditions for the DCTL, RTL and RCTL families. With the EIA registration format as a reference, this discussion is presented to broaden the definition of certain parameters used in selecting monolithic microcircuits.

2. Logic Elements

The basic logic elements used to implement logic functions are the AND, OR, and NOT gates. The NOT element is usually used in combination with the AND and OR to provide a NAND and NOR element. Another element used in logic design is a memory element referred to as a bistable multibivrator or flip-flop. The symbols for the basic logic elements are shown in Figure 1-28.

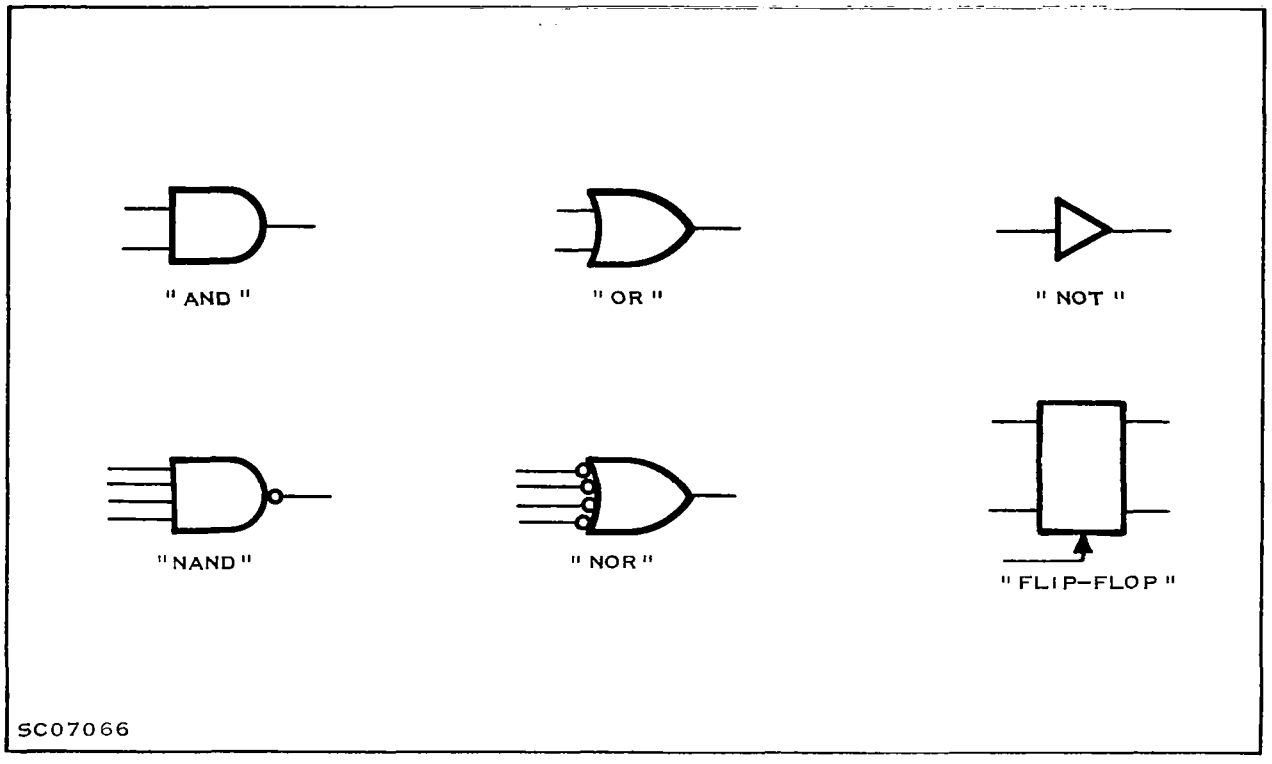


Figure 1-28. Logic Elements

3. Logic Definitions

Two possible logic assignments, positive logic or negative logic, are used to implement a Boolean function. For positive logic, a logical "one" is represented by a "high" voltage level, and a logical "zero" is represented by a "low" voltage. The reverse is used to represent negative logic. The following is a tabular listing of the logic assignments:

Logic Assignment	Binary Voltage Level	
	"0"	"1"
Positive	Low	High
Negative	High	Low

4. Fan-Out

Fan-out is the term used to describe the number of loads that can be driven from a single output. In general, the maximum fan-out is specified on a manufacturer's data sheet by the symbol "N." In system design it is necessary to better define the fan-out capabilities of a circuit in terms of output current that can be supplied or sinked from a single output. For example, the maximum fan-out for a typical TTL gate is

expressed as N = 10. This fan-out reflects the ability of a single output to sink current from 10 identical gates at a logical "0" voltage, and to supply current to 10 identical gates at a logical "1" voltage level. In a typical TTL family this means that a single gate can sink a load current of 16 mA and supply a load current of 400 mA. Defining the fan-out in terms of current is very important when interfacing two different families (i.e., DTL and TTL).

In summary, fan-out of a single output is determined by the input-current requirements of the loads or circuits being driven, and is expressed in terms of equivalent devices that can be connected to a single output.

5. Fan-In

Fan-in is the number of inputs to a logic gating element. Some devices provide increased fan-in by having provisions for the addition of expander circuits; fan-in also can be increased through combinational logic. Expanding the fan-in of a device by using "wired-on" or "expansion inputs" is not recommended when using most monolithic microcircuits, because of noise considerations.

6. Cascade Levels

Cascade levels represent the maximum number of series-connected gates that can be used between clocked flip-flops. The cascade parameter is not used in characterizing a circuit, but it is an important definition in system design. It is not specified on data sheets; however, the parameter-propagation delay time is used to determine the number of series gates required for a given frequency. A typical curve illustrating the maximum cascade levels is shown in Figure 1-29.

7. Propagation Delays

Propagation delay is the parameter most widely used in defining the operating speed of digital circuits. Although the speed of some circuits is characterized by delay and transition times, propagation delay is becoming a more acceptable definition. The propagation delay time is a function of the fan-out and capacitance the output is driving, and it should be tested for the worst-case design condition. Propagation delay times are defined in terms of the following parameters and are measured as indicated in Figure 1-30:

- $t_{pd"0"}$ is the propagation delay time measured with the defined output changing from the defined "one" state to the defined "zero" state.
- $t_{pd"1"}$ is the propagation delay time measured with the defined output changing from the defined "zero" state to the defined "one" state.

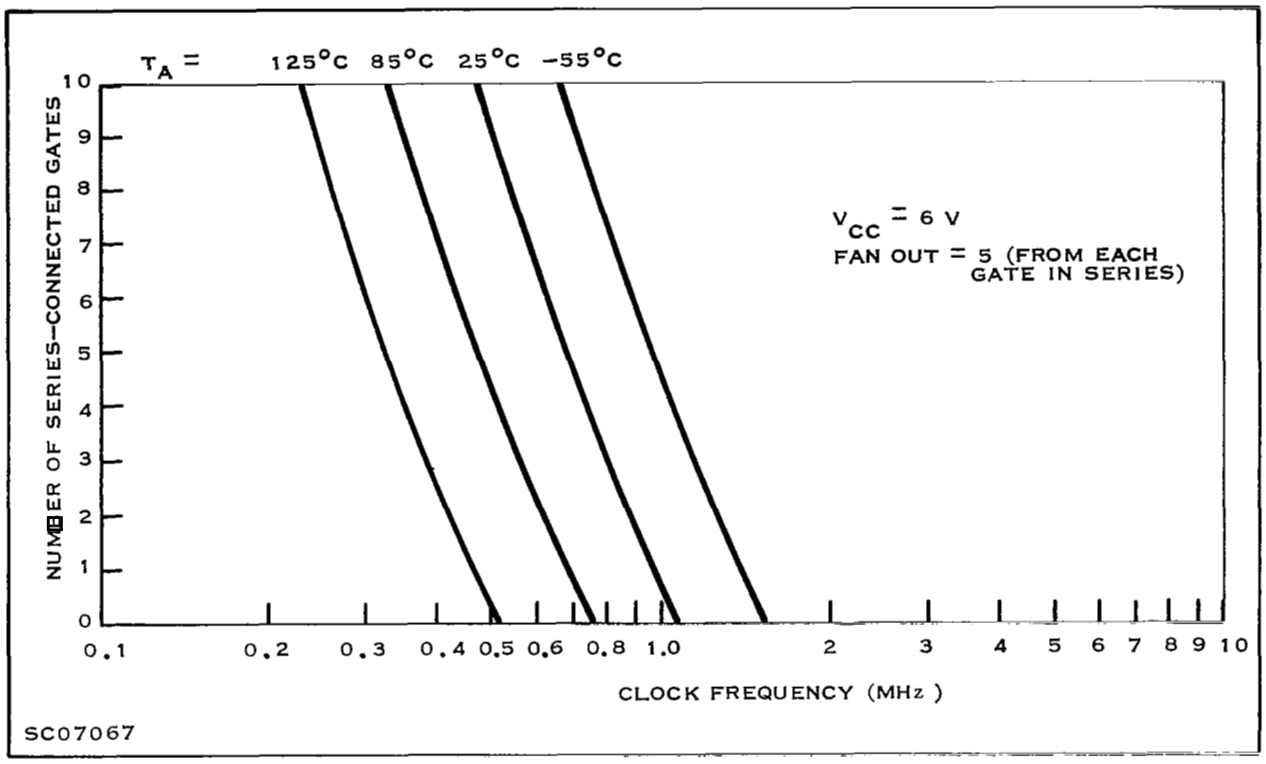


Figure 1-29. Number of Series 51 Gates that Can Be Connected in Series Between Clocked Flip-Flops, versus Frequency of Operation

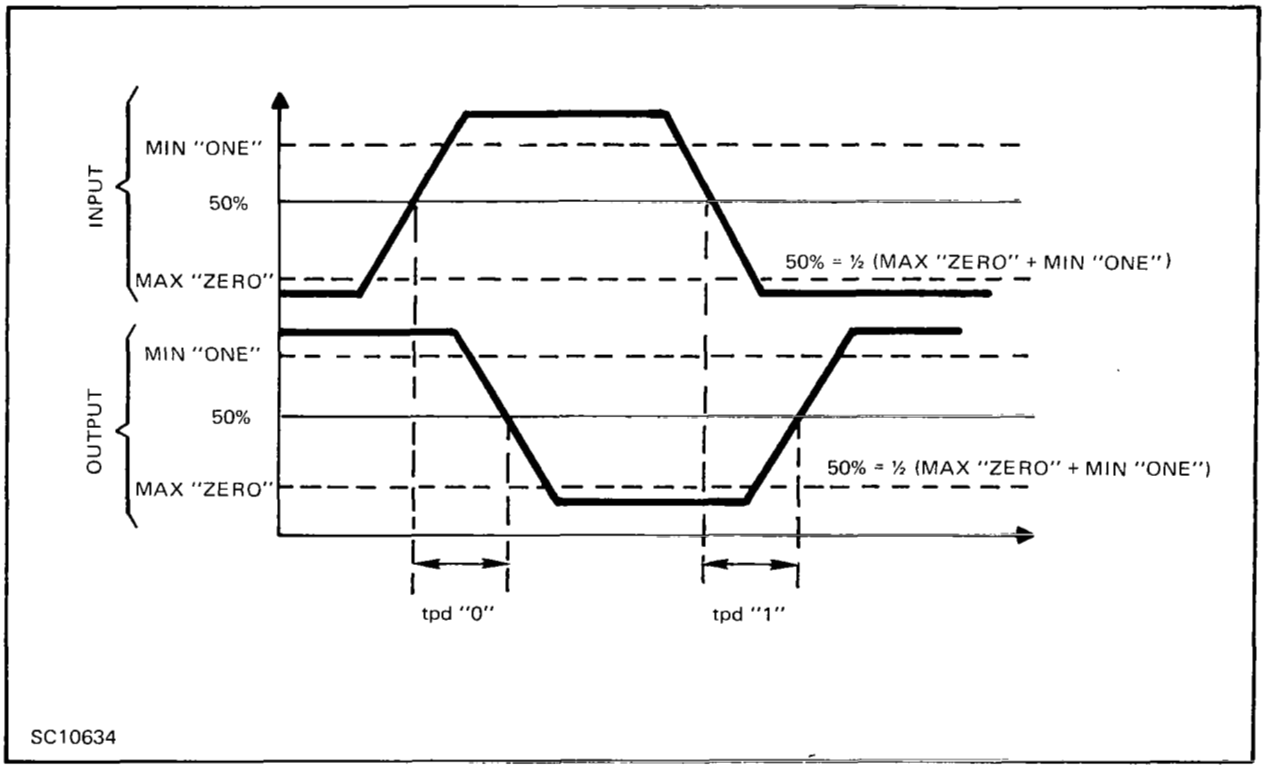


Figure 1-30. Measurement of Propagation Delay

In selecting microcircuits, generally, one cannot consider speed without also taking into account power dissipation. Speed and power are usually evaluated together, since an attempt to achieve higher speed requires an increase in power dissipation.

8. Power Dissipation

Power dissipation for the majority of digital monolithic microcircuits is at a low level (less than 150 mW) compared to the maximum possible dissipation of the circuit die or package. However, the new complex arrays and extremely high speed circuits are having to be placed in larger packages to reduce the temperature rise of the circuit die.

Circuit power requirements are usually measured in terms of supply current at a given voltage. The power dissipation for the majority of circuits will vary with temperature, and will vary between the output's logical "one" and logical "zero" states. The power requirement for gates could increase by a factor of two or three on switching between output logical states; whereas, with flip-flops, the power drain is essentially the same for both states.

9. Noise Immunity

a. General

The subject of noise immunity must be treated in greater detail than simply specifying a certain number of millivolts tolerance to unwanted signals. Specifically, the following must be considered:

- Is the noise of a steady dc nature, or is it an ac noise spike of small time duration?
- Where does the noise appear - on the supply line, signal line, or ground line?
- Is the noise immunity specification a typical number or a guaranteed value?

Each of these questions will be discussed in the analysis to be presented hereafter.

b. AC Noise Immunity

It is difficult to define ac noise, but it is more difficult to relate it to a specification. Generally speaking, dc noise is worst case. With reference to Figure 1-31, which is a plot of noise immunity versus pulse width (pulse width is really the only difference between dc noise and ac noise), it is apparent that the smaller the pulse width the more immune the circuit is to the noise.

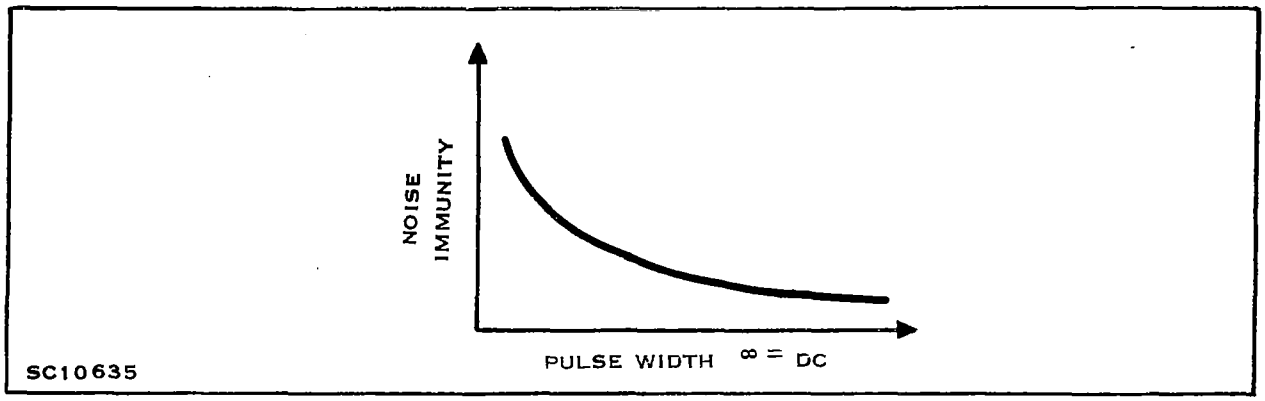


Figure 1-31. AC Noise Susceptability (Noise Immunity versus Pulse Width)

A preferred term when discussing ac noise might be "ac noise susceptability," or how susceptable a circuit is in allowing noise to appear on its input or output. In newer designs the trend is toward the lower impedance, emitter-follower type outputs. In the logical "zero" state these outputs are similar to the conventional transistor with collector pull-up resistor. However, in the logical "one" state the lower impedance of the emitter follower output (< 100 Ω) is more effective in keeping noise from ever appearing on an output, than for example, a conventional DTL output which may have an impedance of up to 6 kΩ. The treatment of noise immunity given here applies to both the low-impedance and the high-impedance outputs, but the more preferable low-impedance output will be demonstrated.

c. DC Noise Immunity

Direct-current noise immunity can be treated in a more difinitive manner than can ac immunity. Variable pulse width and pulse shapes do not need to be considered; the noise can be assumed to be a sustained "battery" noise, independent of time, which appears at a particular location in the circuit.

d. Noise Location

(1). General. It is necessary to discuss the three locations through which external noise can reach a circuit—the supply voltage line, the ground line, and the signal (input-output) line.

(2). Supply Voltage Line. Logical "one" voltage levels on the outputs of logic circuits are influenced primarily by the level of the supply voltage. Referring to a typical output configuration, Figure 1-32, it is seen that in the logical "one" state the output is driven from a circuit which resembles an emitter-follower. Except for the small collector resistor R_1, Q_1 would never saturate and would always act as a true emitter-follower. The expression for the output logical "one" voltage is:

$$V_{out(1)} = V_{CC} - IR_2 - V_{BE(Q_1)} - V_D \quad (1)$$

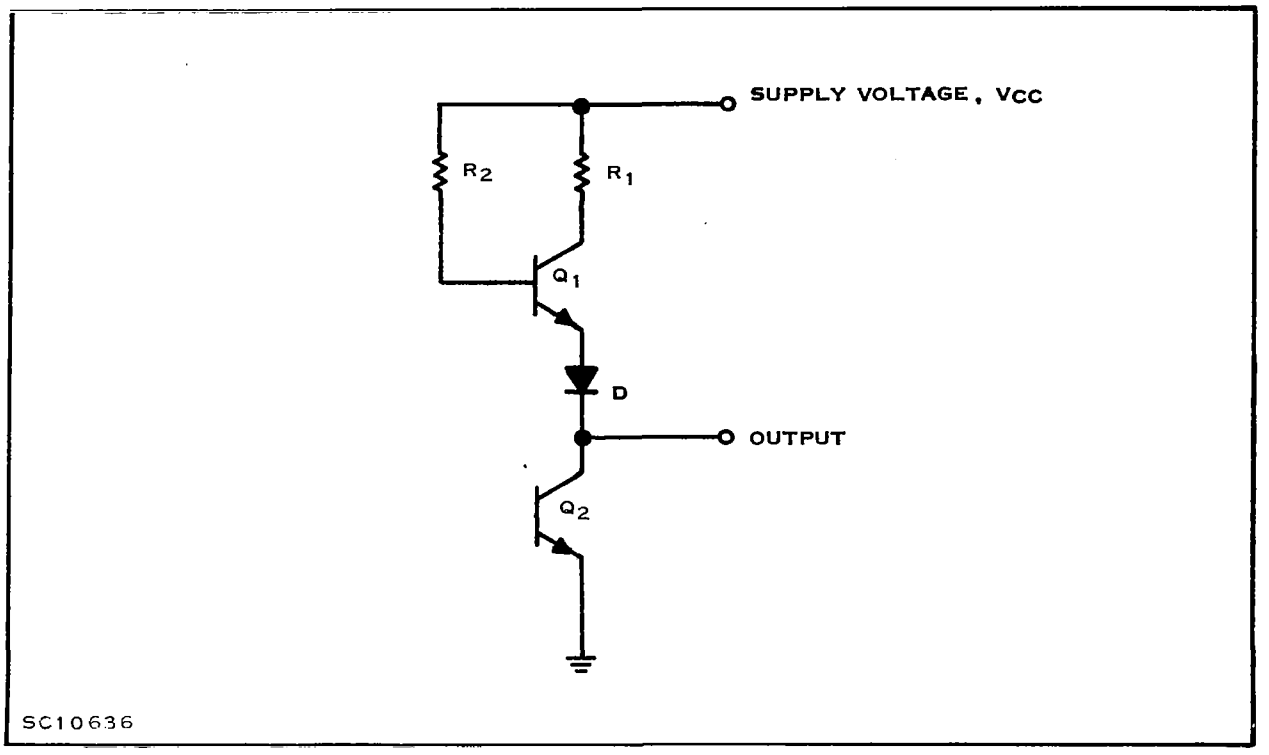


Figure 1-32. Typical Output Circuit
(Illustrating Noise Location)

For small changes in the supply voltage, the values of IR_2, $V_{BE(Q_1)}$, and V_D change only slightly. Thus the output voltage changes practically volt-per-volt with changes in V_{CC}. Therefore, treatment of the effects of noise on the signal line can be related to the supply line as well.

(3). Ground Line. When the output is in the logical "zero" state, transistor Q_2 (Figure 1-32) is fully saturated. Under this condition if the emitter of Q_2 is raised above ground by a noise voltage on the ground line, the collector voltage will increase by the same amount. (It is assumed that sufficient overdrive is available to keep Q_2 in saturation). Therefore, a direct relationship also exists between ground noise and signal line noise. Subsequent discussion of noise immunities will be limited to the signal line only, but it should be remembered that negative-going logical "one" noise and positive-going logical "zero" noise can be related to supply line noise and ground noise respectively.

e. Typical or Guaranteed Noise Immunity

(1). General. In the previous discussion on ac noise immunity, a comparison of equal voltage levels of an ac noise pulse and a dc sustained level will show that the circuit will be less immune to the dc level. Therefore, the worst-case dc conditions will now be considered.

A $V_{in} - V_{out}$ curve for a typical microcircuit gate is shown in Figure 1-33. Although V_{BE} and resistor values change with temperature and thus cause shifts in the $V_{in} - V_{out}$ response, the 25°C condition is shown for demonstration.

(2). Typical Noise Immunity. As seen on the curve (Figure 1-33), this typical gate changes state when approximately 1.4 V is applied in the input. Since the recognition of a binary "one" instead of a desired binary "zero" (or conversely) is the only real cause of dc system error, it is this 1.4-V point on an input which must not be exceeded through noise applied to an input logic signal.

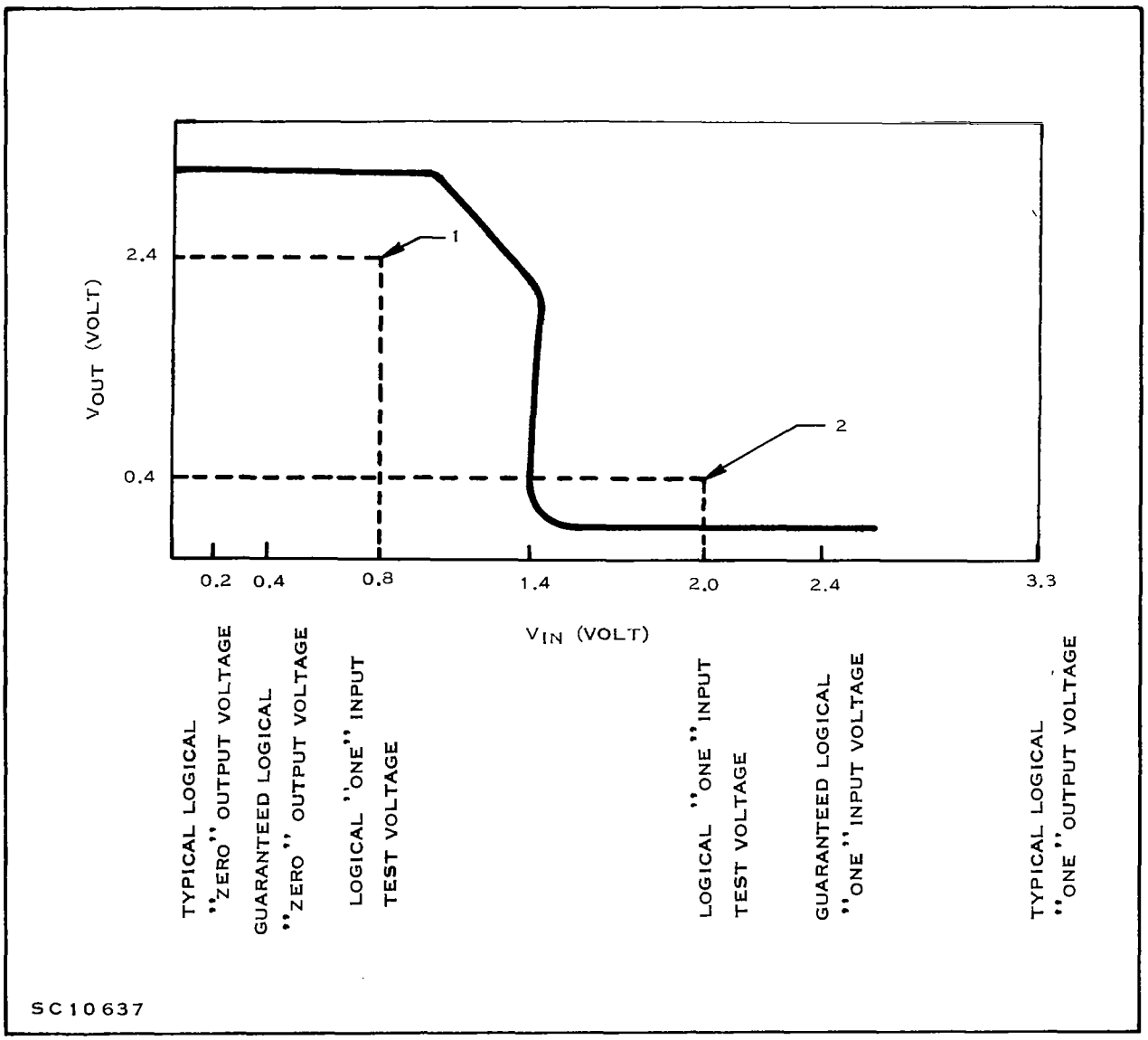


Figure 1-33. Transfer Characteristic of a Typical Gate

Although the 3.3-V point is labeled as a typical output voltage on the curve, it must be realized that the output voltage for one gate is the input voltage for another, as shown in Figure 1-34(a).

Since an output voltage in the "one" state is typically 3.3 V, and since the gate it is driving will not change state until it reaches about 1.4 V, this indicates that 1.9 volts of negative-going noise could appear before an erroneous change of state would occur on the second gate.

A similar situation is true for the logical "zero" condition, as shown in Figure 1-34(b). A typical output voltage (input voltage to the gate it is driving) is 0.2 V.

Before reaching the 1.4 V threshold level, 1.2 V of noise could be applied (Figure 1-34 (b)). Thus it is stated that this gate (Figure 1-33) has, typically, greater than 1-Vdc noise immunity.

(3). Guaranteed Noise Immunity. It is necessary for a design engineer to receive not only a guarantee that a gate will not false trigger, but he must also be guaranteed a specific output voltage when a simulated dc noise level appears at an input.

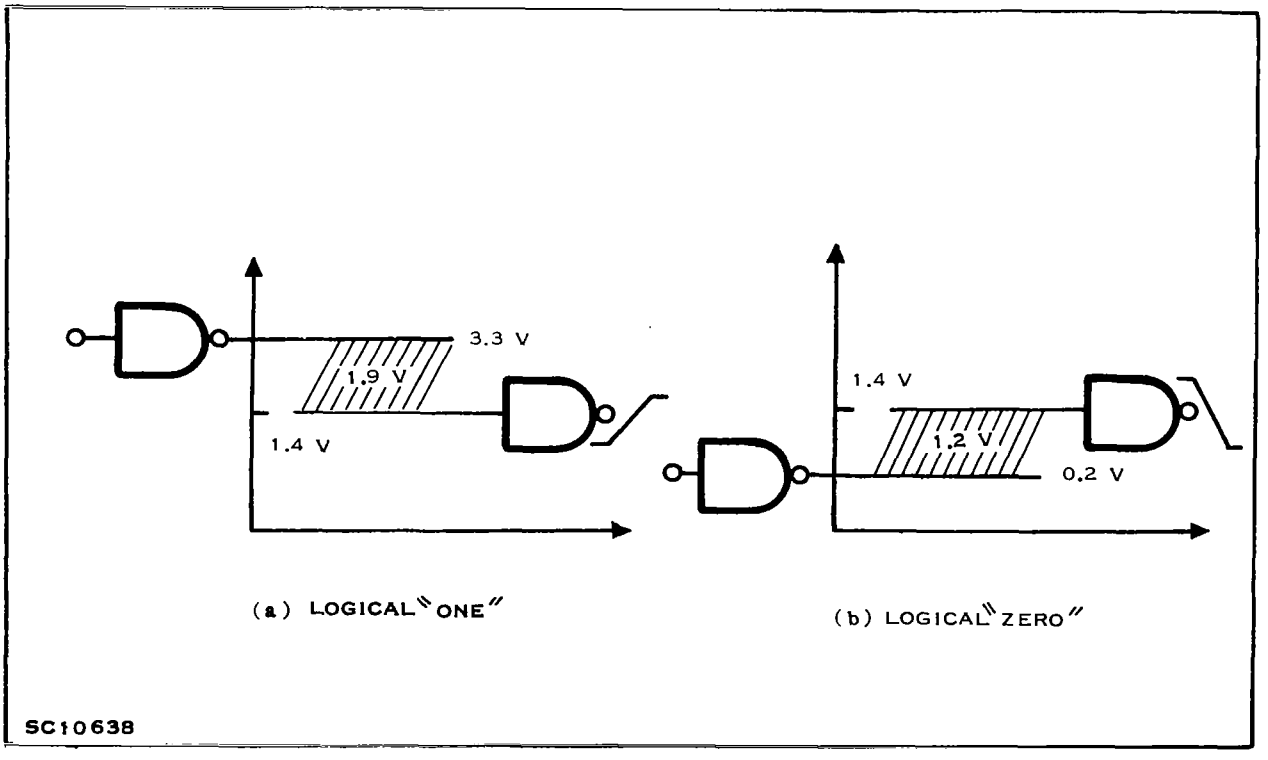


Figure 1-34. Typical Noise Immunity of Logic Gates

First, a guaranteed output voltage must be specified. In the case of one popular TTL line this is 2.4 V. It is truly worst-case when it is measured at the lowest supply voltage, since this produces the lowest logical "one" output voltage. Also, a worst-case condition is assured if loading is maximized while this voltage is measured. The unused inputs should be placed in their worst-case condition when this test is made.

Next an input voltage must be chosen which will produce a voltage lower than the logical "zero" maximum of 0.4 V on the gate's output (Figure 1-35(a)). The threshold voltage of 1.4 V cannot be used as an input voltage, since at the lower temperatures most of the circuits would have output voltages greater than 0.4 V. The value of input voltage chosen was 2.0 V. This insures that 400 mV of negative-going noise can be applied to a 2.4 V output signal, and the resulting 2.0 V feeding another gate's input will still be adequate to keep the second gate's output below the logical "zero" limit of 0.4 V.

Similarly, the same approach is taken in determining a logical "zero" input condition (Figure 1-35(b)). The logical "zero" input voltage is again tested under worst-case conditions of supply voltage, loading, temperature, and unused

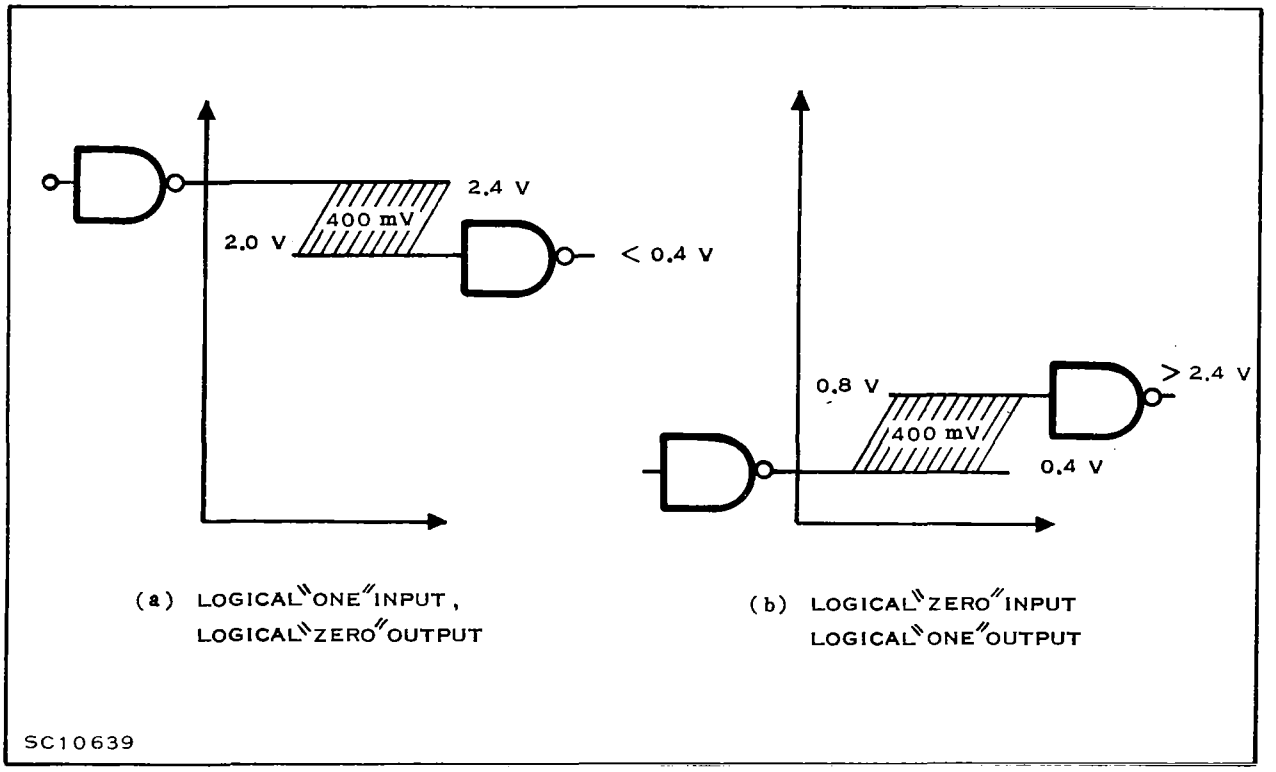


Figure 1-35. Guaranteed Noise Immunity

inputs. A limit of 0.4 V is selected as the limit. To insure the same 400 mV guaranteed noise immunity, a value of 0.8 V was selected as the input test condition which could be applied and still keep the output from falling below its 2.4 V minimum.

Relating the guaranteed dc noise immunity to the $V_{in} - V_{out}$ curve (Figure 1-33), it can be seen that to be able to guarantee a worst-case noise margin:

- The curve must stay above the logical "one" limit until it passes Point 1, and must go beneath the logical "zero" limit before it reaches Point 2, for all conditions of supply voltage, temperature, loading, etc.
- The guaranteed dc noise immunity will be greater the wider the separation between the values of Point 1 on the V_{out} axis and Point 2 on the V_{in} axis, and the wider the separation between the values of Point 2 on the V_{out} axis and Point 1 on the V_{in} axis.

C. SELECTION OF LOGIC CIRCUITS

1. General

The majority of monolithic microcircuit families have been developed for a particular parameter requirement. The selection of a circuit family depends almost entirely upon the requirements of a specific application and system. For each application, the user must evaluate the system requirements, considering such parameters as power dissipation, propagation delay times, operating temperature, and noise immunity, and of course, availability and cost. No one logic family is clearly superior in every parameter to all other families, and basic trade-offs must be made in selecting a particular logic type.

2. Basic Precautions

When selecting a particular family or an individual device, there are some basic precautions that should be observed:

- Don't carry over prejudicies. Don't select a monolithic circuit family just because it is a familiar discrete-component logic scheme. This is a natural tendency that results from the present transition period from discrete-component circuits to monolithic microcircuits. A microcircuit family that does not exist in discrete-component form may offer a much better scheme for the solution of a design problem.

- Know the particular circuit. Don't attempt to use a microcircuit with only "black-box" characteristics as a guide. A design engineer should understand that a network from the same family but made by a different manufacturer may not be equivalent to another manufacturer's product. In unusual applications the designer may find it helpful to gain some knowledge of microcircuit fabrication techniques.

- Know the system Requirements. There are many trade-off possibilities in selecting microcircuit families. Don't choose a family with high speed if it is not needed; it could require unnecessary system power. A better choice might be one of the families that offer compatible gates having different speeds. Thus, for certain functions which require high speed, a faster gate could be used, but for the other system requirements a slower gate with a lower power requirement would be adequate. Don't choose a circuit that operates over the full military temperature range unless this capability is needed. A circuit with a limited temperature range will cost appreciably less.

3. Characterization of Circuit Families

a. General

Monolithic microcircuits involve so many performance considerations and such a complex technology that it makes generalization or characterization of one logic family somewhat difficult, let alone generalization over the wide range of circuit families.

Manufacturers' monolithic digital circuits are grouped by families in Table 1-2. Each table presents the basic characteristics for each manufacturer's one or more series of devices in a given microcircuit family. Very few of the devices of any of the several series shown for a particular family of circuits are interchangeable with those of another series in the same table. One should not select a logic family from the tables shown here or from any general listing of logic circuits. The tables are presented merely to show the number of circuits available. However, any listing such as this one fails to reflect the new products that are being introduced. The list of series does show one basis for investigation of a particular series—the popularity of a series is reflected by the number of circuits contained in that series. This brings up two basic questions that should be answered before selecting a particular family, and then a specific series. What is the history of the circuits? What major projects have used the series, and are they still using them?

Table 1-2. Monolithic Microcircuit Logic Families (From EDN, 1966 Semiconductor Annual) (Sheet 1 of 3)

Logic Family	Manufacturer*	Series	No. of Circuits	Supply (Volt)	Noise Immunity (Volt)	Temperature Range (°C)	Characteristics**
RTL	GME	134	9	3.0 to 4.0	0.08 to 0.25	−55 to 125	CDH
	GME	134	9	3.0 to 4.0	0.08 to 0.25	0 to 75	CDG
	TI	1700	7	3.0	0.15	−55 to 125	CDH
	Mot	MC700	25	3.6	0.3	15 to 55	BDG
	Mot	MC800	15	3.0	0.3	0 to 100	BEG
	Mot	MC900	15	3.0	0.3	−55 to 125	BEH
	Mot	MC908	10	3.0	0.25	−55 to 125	CDH
	Fch	μL900	11	3.0	0.25	−55 to 125	BEH
	Fch	μL900	11	3.6	0.3	15 to 55	BEG
	Spr	μL900-21	11	3.0	0.25	−55 to 125	BEH
	Spr	μL900-22	11	3.0	0.25	0 to 100	BEG
	Spr	μL900-29	11	3.0	0.25	15 to 55	BEG
	Fch	μL908	7	3.0 to 4.0	0.2	−55 to 125	CDH
	Phl	MW/3	10			−55 to 125	BDH
	NSC	NB1000	14	3.0	0.265 to 0.54	−55 to 125	BEH
	NSC	NB2000	14	3.0	0.265 to 0.54	0 to 100	BEG
	NSC	NB3000	14	3.0	0.265 to 0.54	15 to 55	BEG
	NSC	NC1000	6	3.0	0.265 to 0.54	−55 to 125	BDH
	NSC	NC2000	6	3.0	0.265 to 0.54	0 to 100	BDG
	NSC	NC3000	6	3.0	0.265 to 0.54	15 to 55	BDG
	Phl	PL900-21	13	3.0	0.25	−55 to 125	BEH
	Phl	PL900-29	11	3.0	0.25	15 to 55	BEG
	Phl	PL908	18	3.0	0.25	−55 to 125	CDH
	Phl	SUPER	6	3.0		−55 to 125	ADH
	Spg	USO700	7				DI
RCTL	TI	51/51R	16	3.0 to 6.0	0.2	−55 to 125	CDH
	Spg	USO100	16	3.0 to 6.0		−55 to 125	CDH
DTL	Aml	001	5	4.0	0.8	−55 to 125	CDH
	Fch	100	6	5.5	0.35 to 0.4	−55 to 125	CFH
	GME	200	26	4.0, −2.0	1.0	−55 to 125	BFH
	GME	200	26	4.0, −2.0	1.0	0 to 75	BFG
	RI	200	7	4.5 to 5.5	0.8	−55 to 125	AEH
	RI	300	7	4.5 to 5.5	0.8	−55 to 125	AEH
	RI	500	7	4.5 to 5.5	0.8	0 to 75	AEG
	SWM	700	3			−55 to 125	
	ITT	930	9			−55 to 125	CEH
	RCA	2200	3	3.8 to 6.3	1.2	−55 to 125	CDH
	TI	15830	11	4.5 to 5.5	0.75	0 to 70	BDG
	TI	15930	11	4.5 to 5.5	0.75	−55 to 125	BDH
	GI	A	15				
	Scx	A01	16	5.0	0.9	−55 to 125	BDH
	Scx	A41	16	5.0	0.9	0 to 70	BDG
	Mot	MC200	14	2.0, 4.0	0.5	−55 to 125	BEH
	Mot	MC250	14	2.0, 4.0	0.5	0 to 75	BEG
	Fch	μL930	11	4.5 to 5.5	0.6 to 1.0	0 to 70	CEG

Table 1-2. Monolithic Microcircuit Logic Families (From EDN, 1966 Semiconductor Annual) (Sheet 2 of 3)

Logic Family	Manufacturer*	Series	No. of Circuits	Supply (Volt)	Noise Immunity (Volt)	Temperature Range (°C)	Characteristi
DTL (Contd.)	Fch	μL930	11	4.5 to 5.5	0.6 to 1.0	−55 to 125	CEH
	Fch	μL9000	3			−55 to 125	CDH
	Gl	NC	7	4.2, 12		−55 to 125	BFH
	Sgn	NE100	35	4.0	1.0	0 to 70	BDG
	Spg			4.0, −2.0			
	Sgn	NE400	2	4.0	0.4 to 0.6	0 to 70	CDG
	Spg						
	Gl	PC	11	4.2, 12		−55 to 125	BFH
	Phl	PL930-51	10	4.0 to 6.0	0.6 to 1.0	−55 to 125	CEH
	Phl	PL930-59	10	4.0 to 6.0	0.6 to 1.0	0 to 75	CEG
	Ray	RM	17	6.0	0.55	−55 to 125	CDH
	Sgn	SE100	35	4.0	1.0	−55 to 125	BDH
	Spg			4.0, −2.0			
	Sgn	SE400	2	4.0	0.4 to 0.6	−55 to 125	CDH
	Spg						
	Scx	S1930	9			−55 to 125	CEH
	Scx	S1930D	9			0 to 70	CEG
	Sgn	SP600	6	4.5	0.5 to 1.0	15 to 55	CEG
	SWM	SW930	9	3.5 to 6.0	0.7	−55 to 125	CEH
	SWM	SW930	9	3.5 to 6.0	0.7	0 to 75	CEG
	Spg	UC1000	6	6.0, −3.0	±0.5	−55 to 125	BFH
	Wst	WM200	28	6.0	0.55 to 1.0	−55 to 125	BEH
	Wst	WM600	4	4.5	0.75 to 1.0	−55 to 125	BEH
	Wst	WS800	8			0 to 125	CEG
Mod. DTL	TI	53	14	3.0 to 4.0	0.3	−55 to 125	BEH
	TI	73	14	3.0 to 4.0	0.3	0 to 70	BEG
	Mot	MC830	16	5.0	0.5	0 to 75	CEG
	Mot	MC930	16	5.0	0.5	−55 to 125	CEH
TTL	SWM	54	8			−55 to 125	BEH
	TI	54	16	4.5 to 5.5	1.0	−55 to 125	BEH
	TI	54-930	7	4.5 to 5.5	1.0	−55 to 125	BEH
	TI	54H	8	4.5 to 5.5	1.0	−55 to 125	AEH
	SWM	74	8			0 to 75	BEG
	TI	74	17	4.75 to 5.25	1.0	0 to 70	BEG
	TI	74-930	7	4.75 to 5.25	1.0	0 to 70	BEG
	TI	74H	8	4.75 to 5.25	1.0	0 to 70	AEG
	Fch	100	2	5.5	0.4	−55 to 125	BEH
	SWM	700	3			0 to 75	
	Scx	Bol	2	5.0	0.7	−55 to 125	BEH
	Tns	HLTTL	73	4.5 to 5.0		−55 to 125	BEH
	Tns	HLTTL	73	4.5 to 5.0		0 to 75	BEG
	Tns	HLTTL	12	4.5 to 5.0	1.0	15 to 55	BEG
	Tns	HLTTL	15	5.0	1.3	0 to 75	BFG
	Fch	μL9000	12			−55 to 125	BEH
	Phl	MEL	3	3.0	0.25	−55 to 125	CDH
	Sgn	NE400	2	4.0	0.4 to 0.6	0 to 70	CDG

ble 1-2. Monolithic Microcircuit Logic Families (From EDN, 1966 Semiconductor Annual) (Sheet 3 of 3)

ogic mily	Manufacturer*	Series	No. of Circuits	Supply (Volt)	Noise Immunity (Volt)	Temperature Range (°C)	Characteristics**
'TL	Spg						
:ont)	Sgn	NE800	9	5.0	1.0	0 to 70	BEG
	Sgn	SE400	2	4.0	0.4 to 0.6	−55 to 125	CDH
	Spg						
	Sgn	SE800	9	5.0	1.0	−55 to 125	BEH
	Syl	SUHL I	38	5.0	±1.0	−55 to 125	BEH
	Syl	SUHL I	38	5.0	±1.0	0 to 75	BEG
	Syl	SUHL II	18	5.0	1.0, −1.5	−55 to 125	AEH
	Syl	SUHL II	18	5.0	1.0, −1.5	0 to 75	AEG
	SWM	SWF	9	5.0	±1.0	−55 to 125	FH
	SWM	SWF	9	5.0	±1.0	0 to 75	FG
	SWM	SWG	18	5.0	±1.0	−55 to 125	BEH
	SWM	SWG	18	5.0	±1.0	0 to 75	BEG
:CL	TI	70	2	1.25, −3.5	0.25	0 to 70	AFG
	Fch	100	2	5.5		−55 to 125	AFH
	SWM	300	11	−10	0.4	−55 to 125	AFH
	SWM	300	11	−10	0.4	0 to 75	AFG
	RCA	2100	2	−4.68 to −5.72	0.32	−55 to 125	AFH
	RCA	2100	3	−4.5 to −5.5	0.33	10 to 60	AFG
	Mot	MC300	16	−1.5, −5.2	0.4	−55 to 125	AFH
	Mot	MC350	16	−1.5, −5.2	0.4	0 to 70	AFG
	Wst	WS300	2				AF

Names of manufacturers are arranged alphabetically as follows:

Abbreviation	Manufacturer	Abbreviation	Manufacturer
Aml	Ameloo Semiconductor	Ray	Raytheon Co.
Fch	Fairchild Semiconductor	Sgn	Signetics Corp.
GI	General Instrument Corp.	Scx	Siliconix, Inc.
GME	General Micro-Electronics, Inc.	Spr	Sperry Semiconductor
ITT	ITT Semiconductor	Spg	Sprague Electric Co.
Mot	Motorola Semiconductor Products, Inc.	SWM	Stewart-Warner
NSC	National Semiconductor Corp.	Syl	Sylvania Electric Products, Inc.
Phl	Philco Corp.	TI	Texas Instruments Incorporated
RI	Radiation, Inc.	Tns	Transitron Electronic Corp.
RCA	Radio Corp. of America	Wst	Westinghouse Electric Corp.

Characteristics

Propagation Delay: A. < 10 nanosec., B. 10 - 30 nanosec., C. > 30 nanosec.,

Power Dissipation: D. <10 m watts, E. 10 - 3- m watts, F. >30 m watts,

G. Industrial, H. Military

b. Summary of Circuit Families

A summary of the circuit families will now be presented. A selection chart based on primary and secondary system design requirements is shown in Table 1-[illegible] The summary of circuit families is as follows:

- Direct-coupled transistor (DCTL) logic is not used presently in monolithic form because of its current-hogging characteristic.
- Resistor-transistor logic (RTL) is probably the lowest cost series on the market today; gates priced as low as 20 cents each, and flip-flops as low as one dollar each are available for commercial use. However, RTL is being phased out in new designs in favor of a series with better power-speed ratio and improved noise immunity. Because RTL is relatively easy to manufacture, it will be used in the intercircuitry of complex arrays, with interfacing provided by other types of circuitry (such as TTL).
- Resistor-capacitor-transistor logic (RCTL) is still being used in high-reliability, low-power, low-speed applications, but, it is giving way to some of the newer series that are more economical to manufacture.
- Diode-transistor logic (DTL) is currently a popular monolithic microcircuit family. It is the first series to become available from several second sources. The DTL 930 series is produced by several of the major manufacturers. All of the entries in this series are electrically interchangeable; however, among some of the manufacturers there are differences in the sizes of the flat-pack packages which they offer as compared with competing product lines in this series.
- Transistor-transistor logic (TTL or T^2L) is considered to be the monolithic microcircuit of the future. Designed originally to provide drive to long lines or capacitive loads, it has also shown that it has several advantages over other families. For instance, TTL provides very good power-speed ratio, good noise immunity, and its manufacturing cost is, or soon will be, lower than that of any other family Much work is being done on the TTL family to broaden its application. To aid designers in achieving optimum system design, several manufacturers are supplying compatible

series that have different power-speed relationships. Some TTL series are approaching speeds of the ECL series, and other TTL series are providing lower power than RTL and RCTL. As with the DTL, several interchangeable TTL series are available from different manufacturers.

- Emitter-coupled logic (ECL) has much to offer when speed is the primary requirement. Although ECL is being used in several applications, its main disadvantage is that it requires at least two power supplies, and in some cases a third precisely regulated, reference supply.

Several special circuit families are not discussed here because they were designed for a particular requirement and thus have not met with wide acceptance. They should not necessarily be overlooked for special applications. However, the families presented here represent the standard monolithic microcircuits presently available.

Table 1-3. A Guide for the Selection of a Microcircuit Logic Family (Based on System Primary and Secondary Requirements)

Priority of Requirement		Design Preference
Primary	Secondary	
Noise Immunity	Speed	TTL
	Low Power	DTL
Speed	Optimum Speed	ECL
	Low Power	TTL or DTL
	Noise Immunity	TTL
Low Power	Speed	RTL or RCTL
	Noise Immunity	DTL
Manufacturing Cost	Noise Immunity	TTL
	Speed	TTL or RTL
	Low Power	RTL or DTL

D. EXAMPLES, ANALYSES AND SPECIFICATIONS OF DIGITAL CIRCUITS

1. General

The following examples of digital monolithic microcircuits represent the three major families that are being used in actual systems. Although only a basic gating element is presented, they serve to illustrate the other gates within each family. Data sheets are used in describing the circuits and for discussing their electrical characteristics.

Several types of flip-flops are presented. They cover the R-S flip-flop, the J-K flip-flop, the relatively simple RCTL flip-flop, which is similar to the common ac coupled discrete flip-flop, and the newer master slave flip-flop which cannot be duplicated economically in discrete form.

2. RCTL Type Circuits

a. Gate

(1). Circuit Description. A basic RCTL gating circuit is shown in Figure 1-36. The two input terminals, labeled A and B, are resistance-capacitance coupled to the gating transistors Q_1 and Q_2, respectively. The output voltage, developed across the common collector resistor, R_3, is used directly as the collector output (C) and is also applied to the complimentary emitter-follower output (C*), consisting of Q_3 and Q_4. Transistor Q_5 is used to provide a low output offset voltage and to decrease the fall time of the output waveform.

(2). Circuit Analysis. An analysis of the operation of the RCTL gate will now be presented. When the two input signals are low so that both Q_1 and Q_2 are turned "off," the output at C will appear as a "high" output. In this case, Q_3 will be turned "on," and Q_4 and Q_5 will be turned "off." When either A or B goes "high," such that one of the gating transistors is turned "on," the resulting output at C or C* will be "low."

The emitter-follower output is not standard to all gates; it is shown here to explain the action of the circuit. Those gates which do not have emitter-follower outputs must be carefully loaded. The input to an RCTL gating circuit appears as a current sink, with a series input resistance of about 20 kΩ. Because of the relatively high resistance of the collector resistor, (in the order of 3.6 to 4.8 kΩ) the

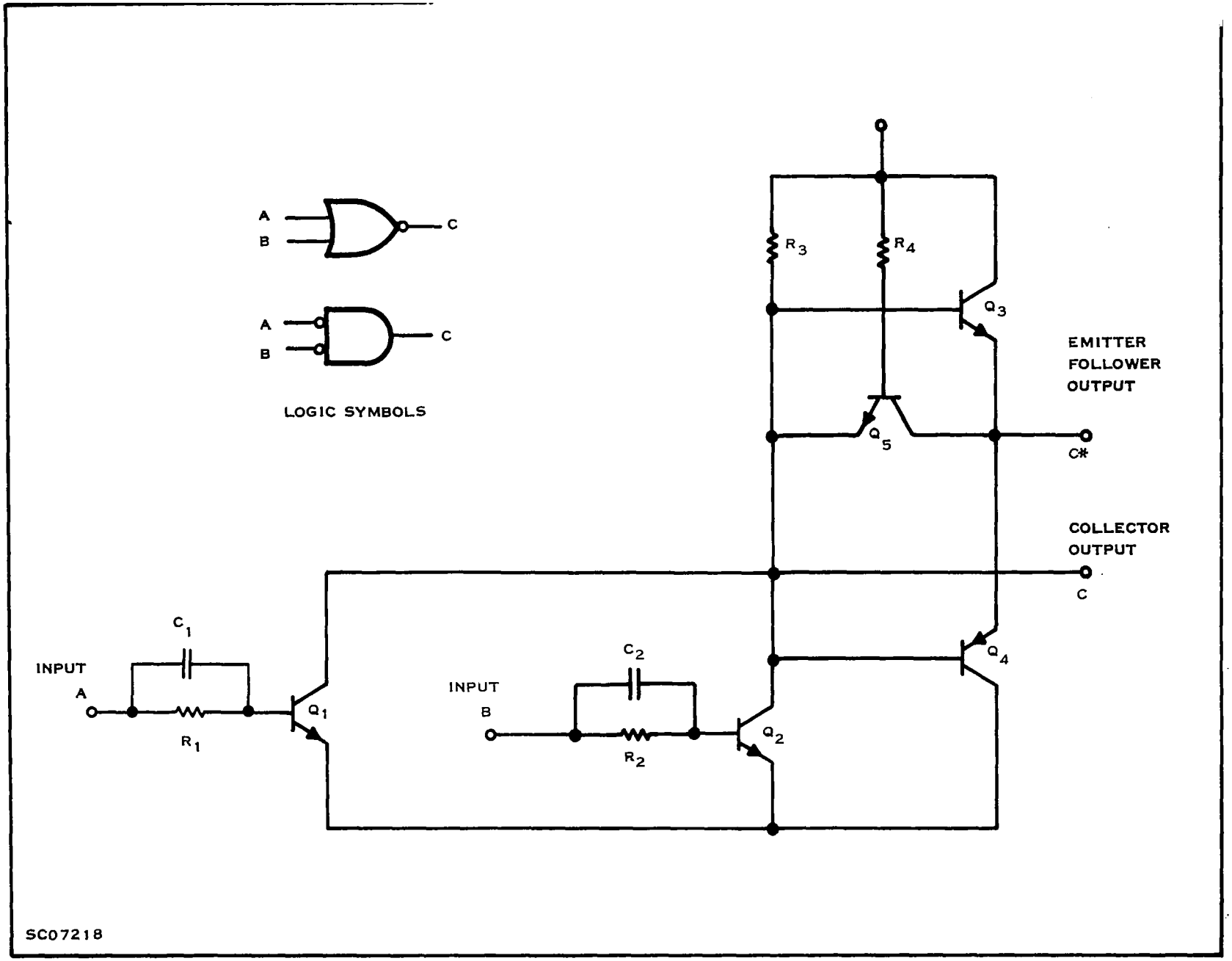


Figure 1-36. Schematic of an RCTL Gate

collector output is limited to driving only a few gate loads; however, in many cases, this is sufficient. If more loads are required, the emitter-follower output can be used. This output provides a low-impedance source in both the logical "1" and "0" conditions and is capable of driving approximately five times the capacity of the collector output. Specific loading characteristics can be found in the data sheet.

The logic equations for this circuit are as follows:

$$C = \overline{A + B} \tag{2}$$

or

$$C = \bar{A} \cdot \bar{B} \tag{3}$$

The first of these two equations presents the gate as a positive logic NOT-OR or simply, NOR gate, while the second equation uses negative logic to provide a NOT-AND or NAND gate. Thus, the gate can be used as either a NAND or NOR gate, depending on whether the logic convention is positive or negative. The truth tables shown in Table 1-4 summarize the logic operation of this circuit.

Table 1-4. Truth Tables for RCTL Gate

Input A	Positive Logic (NOR Gate) Input B	Output C or C*
0	0	1
0	1	0
1	0	0
1	1	0
Input A	**Negative Logic (NAND Gate) Input B**	**Output C or C***
0	0	1
1	0	1
0	1	1
1	1	0

(3). Use of the Data Sheet

(a). General. A data sheet for an RCTL gate is shown in Figure 1-37. These data are for a six-input gate that is designated SN512B or SN513B, depending on whether or not it is equipped with an emitter-follower output.

TYPES SN 512, SN 513
SOLID CIRCUIT® DIFFUSED SILICON "NOR" OR "NAND" LOGIC NETWORK

NETWORK CHARACTERISTICS

absolute maximum ratings

Supply Voltage	8 Volts
Input Voltage	8 Volts
Operating Ambient Temperature Range	−55°C to +125°C
Storage Temperature	−55°C to +125°C

network electrical characteristics	V_{CC} = 3V Min	Typ	Max	V_{CC} = 6V Min	Typ	Max	Units
✳Network Dissipation (ON Condition; T_A = 25°C)		2			7		mw
✳Loading							
Fan-In (NOTE 1)			6			6	
Output G on SN 512 and SN 513 DC Fan-Out (NOTE 2)			5			5	
Output H* (Emitter Follower — available only on SN 513) DC Fan-Out			25			25	
Input Voltage That Will Ensure Turn-On At Any Input Terminal:							
(T_A = 125°C)	1.15			2.0			Volts
(T_A = −55°C)	1.6			2.5			Volts
Input Voltage That Will Ensure Turn-Off At All Input Terminals:							
(T_A = 125°C)			0.22			0.30	Volts
(T_A = −55°C)			0.40			0.50	Volts
Output Voltage							
Output G on SN 512 and SN 513 (NOTE 3)							
OFF Level (T_A = 125°C; N = 0)	2.5			5.0			Volts
(T_A = 125°C; N = 5)	1.15			2.0			Volts
(T_A = −55°C; N = 5)	1.60			2.5			Volts
ON Level (T_A = 125°C)			0.22			0.30	Volts
(T_A = −55°C) (NOTE 4)			0.40			0.50	Volts
Output H* (SN 513 Only)							
OFF Level (T_A = 125°C; N = 25)	1.8			3.8			Volts
ON Level (T_A = 125°C)			0.22			0.30	Volts
switching time (T_A = 25°C; N = 1) (NOTE 5)	(Pulse Amp = 2v)			(Pulse Amp = 4v)			
f = 40 KC, PW = 5 μsec, t_f = 100 nsec							
Delay Time (t_d)		130	170		70	130	nsec
Rise Time (t_r)		150	200		85	150	nsec
Storage Time (t_s)		75	130		75	110	nsec
Fall Time (t_f)		1.2	1.6		1.0	1.4	μsec
Time to Reach a Voltage to Set a Flip-Flop (t_f') (NOTE 6)		350	550		350	550	nsec
Propagation Delay; (t_p) Output G		150			65		nsec
Propagation Delay; (t_p) Output H✳		175			90		nsec

NOTE 1: A Fan-In of 12 per logic stage is possible by connecting two "G" output terminals in parallel and leaving one of the supply voltage terminals (pin 3) disconnected. DC Fan-Out at 125°C reduces by 2 for each SN 512 in parallel.

NOTE 2: AC Fan-Out: When fanning-out into flip-flop clock pulse inputs (AC Load) the emitter-follower output on the SN 513 should be used for fan-outs above 5 or frequencies above 500 KC.

NOTE 3: Inputs: at 125°C, V_{in} = 0.22v for V_{CC} = 3v, V_{in} = 0.30v for V_{CC} = 6v; at −55°C, V_{in} = 0.40v for V_{CC} = 3v, V_{in} = 0.50v for V_{CC} = 6v.

NOTE 4: Each input tested separately: at 125°C, V_{in} = 1.15v for V_{CC} = 3v, V_{in} = 2.0v for V_{CC} = 6v; at −55°C, V_{in} = 1.6v for V_{CC} = 3v, V_{in} = 2.5v for V_{CC} = 6v.

NOTE 5: Switching time variations can be approximated from the curves showing propagation delay vs temperature using the same percentage change between two ambient temperatures.

NOTE 6: This is the delay time necessary to steer a zero into either the R or S inputs of a flip-flop.

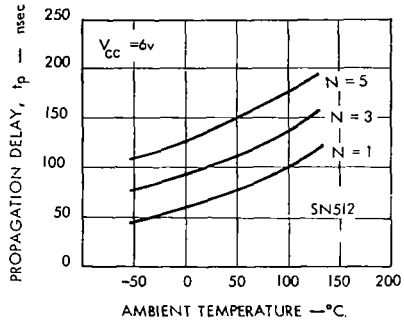
TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

SC07265(1-2)

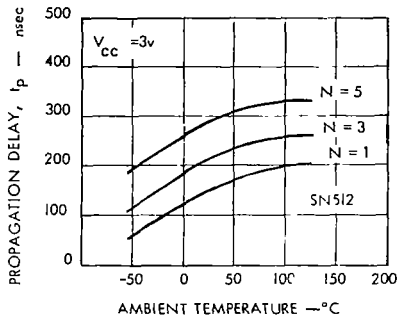
Figure 1-37. Data Sheet for a Six-Input RCTL Gate (Types SN512, SN513) (Sheet 1 of 2)

TYPICAL CHARACTERISTICS

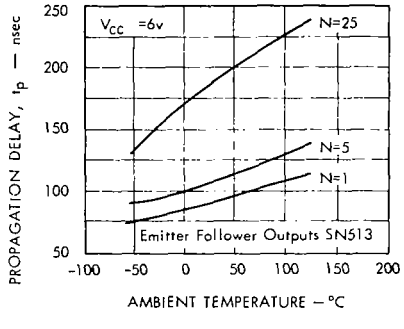
✱ PROPAGATION DELAY .vs TEMPERATURE



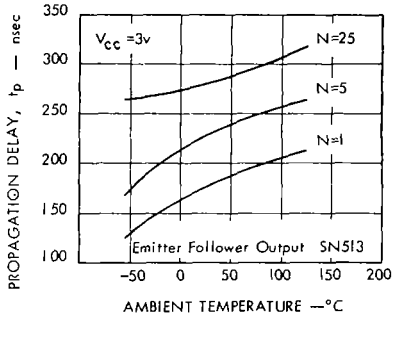
✱ PROPAGATION DELAY vs TEMPERATURE



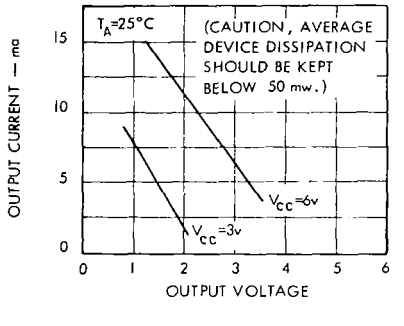
✱ PROPAGATION DELAY vs TEMPERATURE



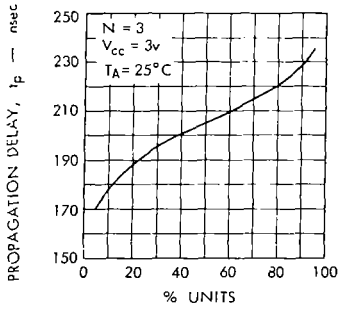
✱ PROPAGATION DELAY vs TEMPERATURE



EMITTER FOLLOWER OUTPUT CHARACTERISTICS



PROPAGATION DELAY vs °₀ UNITS



TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

SC07265(2-2)

Figure 1-37. Data Sheet for a Six-Input RCTL Gate (Types SN512), SN513) (Sheet 2 of 2)

If the device is to be interconnected within the same device family (only RCTL circuits) and is not to be used as an interface with discrete component circuits, the most useful electrical characteristics on the data sheet are propagation delay, loading, and power.

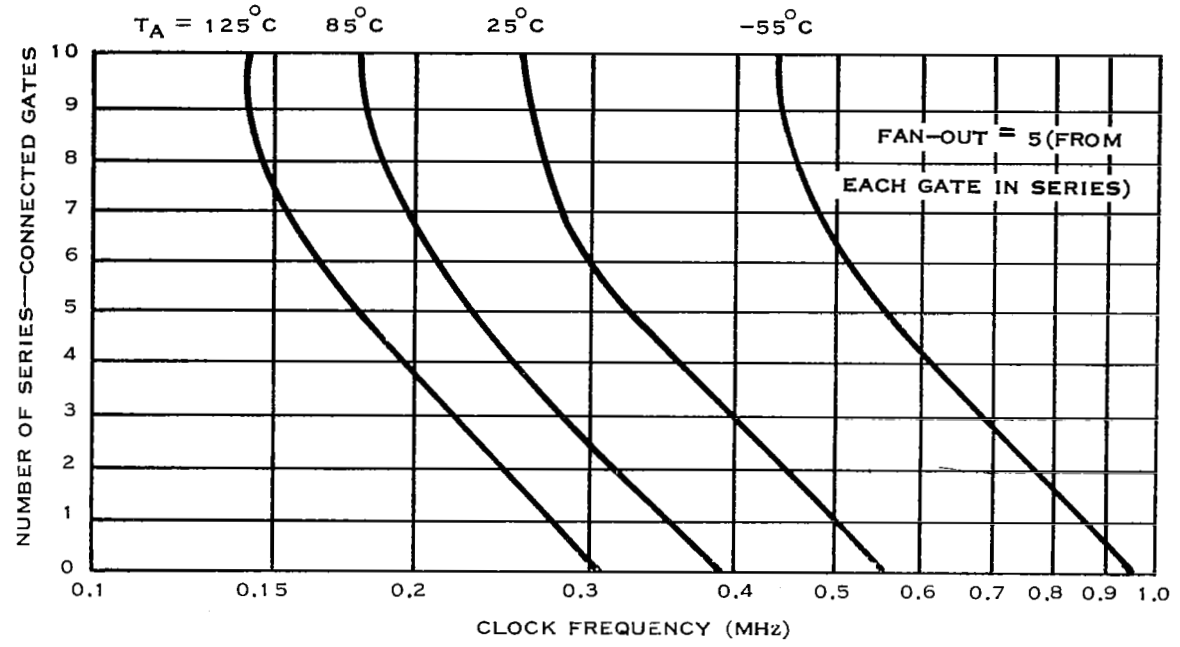
(b). Power. As shown in the data sheet, the device is specified for 3-V and 6-V supply voltages (V_{CC}). Although the maximum rating is given as 8 V, the useful operation of the circuits should fall between the 3-V and 6-V limits. Within these limits, the device is designed to operate compatibly with the other RCTL devices. It is not intended to be "derated" by operating at a lower supply voltage. The supply voltage need not be precisely regulated, but it should be well filtered to prevent switching transients from upsetting the operation of the various logic elements.

Power dissipation is specified for the "on" condition at room temperature ($T_A = 25°C$). One should be aware that most of this power is dissipated in the diffused silicon resistors of the circuit. This being the case, it can be expected that the power will be a function of temperature, in accordance with the temperature-resistance characteristics of silicon. For this reason, it is not uncommon for the system power requirements to increase 20-to-30 percent when operated at $-20°C$, and to decrease approximately that amount at $+80°C$.

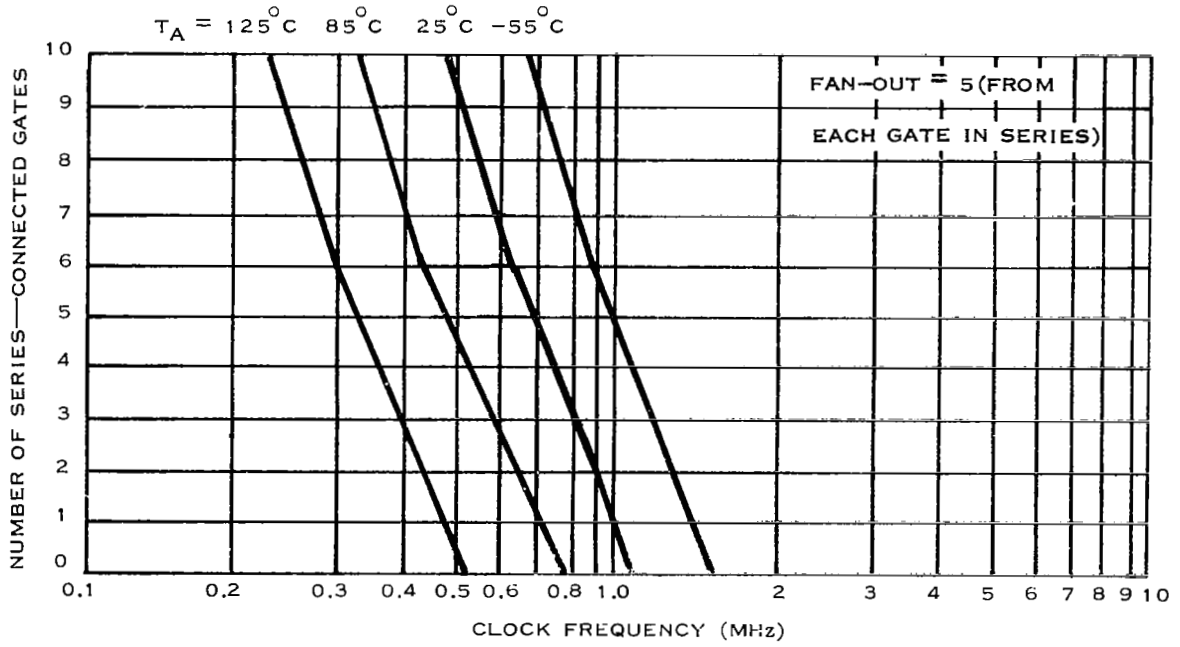
(c). Propagation Delay. Both supply voltage and temperature play an important role in the propagation delay of the gate. In general, the delay decreases with higher supply voltage and lower temperatures. For this reason, the choice of the supply voltage may well depend upon the speed at which the system is required to operate. It can be noted in the propagation delay curves that loading also affects this characteristic. Increased loading lengthens the delay.

Data on propagation delay can be presented graphically in a manner similar to that of Figure 1-38(a) and Figure 1-38(b). These graphs give a more direct relationship of the number of gates which can be connected in series between clocked flip-flops, plotted as a function of temperature and frequency of operation. The compilation of data was made with the consideration that collector outputs on the gates are used and that there is a load of five on each gate. Maximum clock-pulse frequencies will increase (average propagation delay will decrease) if the fan-out is less than five from each gate. Also, a clock-pulse frequency increase of 10-to-20 percent can be realized if emitter-follower outputs are used.

(d). Loading. The loading characteristics are extremely important for the proper operation of the circuit. Overloading the collector output will lower this output in the "off" condition and perhaps prevent the following gates from being properly saturated.



A. V_{CC} = 3.0 V



B. V_{CC} = 6.0 V

SC07267

Figure 1-38. Number of Series 51 Gates that can be Connected in Series Between Clocked Flip-Flops, versus Frequency of Operation

The data sheet for this device indicates that a maximum of 5 loads can be connected to the collector output,and a maximum of 25 loads for the emitter-follower. These loads represent the dc fan-out of the device. To calculate dc loading, all gate inputs, the reset, set, preset, or clear inputs of the flip-flop are considered to be dc loads. A typical input of this type can be represented by a parallel combination of a 20 kΩ resistor and a 50 pF capacitor, both connected in series with a 1N914 diode. This circuit is shown in the data sheet. When the output drives the clock pulse input of a flip-flop, ac loading occurs. The effect of this added capacitance (approximately 100 pF per clock-pulse-input) limits ac fan-out to a maximum of 5. If maximum dc fan-out of the emitter-follower is used, fan-out of the collector output is not available.

(e). Other Applications. If the device is to be interconnected with discrete-component circuitry or with other microcircuits (DTL, TTL), attention must be given to the other electrical characteristics shown in the data sheets. Among these are the input voltage that will insure turn-on and turn-off. The data on the output voltage will be of interest if the output of the device is to be loaded with transistor circuits. The emitter-follower output characteristics are given in a data-sheet graph of the output current versus the output voltage, along with a statement of the maximum power output.

(f). Special Notes. If any inputs to the gate circuit are unused, they should be connected to circuit ground. This will prevent noise and leakage from inadvertently turning the gate "on."

The construction of this gate causes a diode junction to exist between the input terminals and circuit ground or V_{CC}. Depending upon the particular device, forcing the input below ground or above V_{CC} will forward-bias this diode and possibly cause damaging current to be drawn. This diode is not shown on the gate's equivalent circuit.

b. Set-Reset Flip-Flop

(1). Circuit Description. The RCTL flip-flop is shown in Figure 1-39. This is a synchronous device with a clock-pulse input. The steering inputs are labeled R and S. The outputs are Q and $\overline{Q}$, (sometimes designated "1" and "0"), with Q* and $\overline{Q}$* available as emitter-follower outputs. Also shown in this circuit are "preset" and "clear" inputs for setting the logic state of the device.

The truth table for this flip-flop is shown in Table 1-5. In discussing the flip-flop, negative logic will be used. That is to say, a logical "1" will be a "low" voltage and a logical "0" will be "high." The truth table shows the condition of the set (S) and reset (R) inputs prior to the clock pulse (t_n), and then the condition of the Q output after the clock pulse (t_{n+1}).

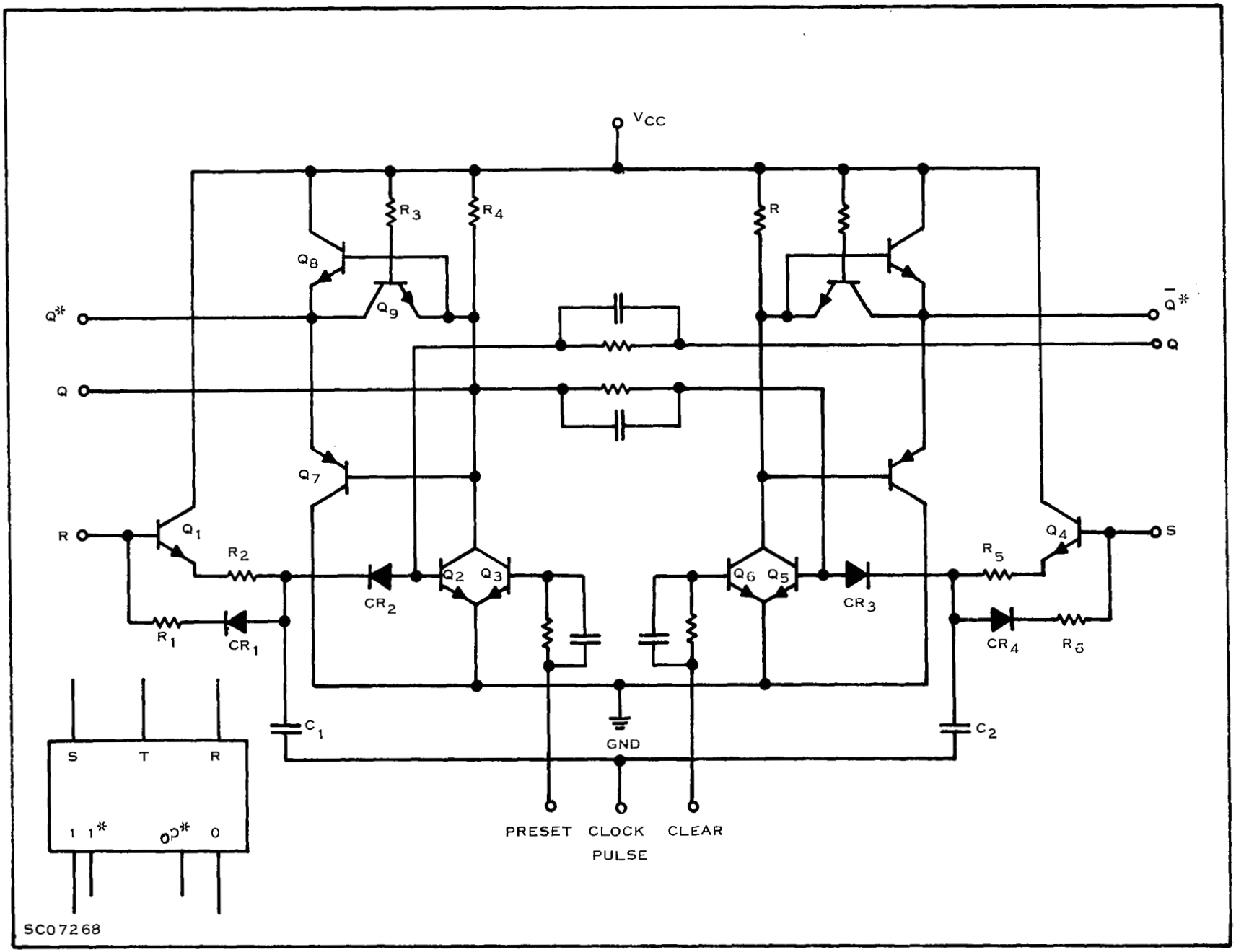


Figure 1-39. Schematic of RCTL Type R-S Flip-Flop

Table 1-5. Truth Table for Type R-S Flip-Flop

t_n		t_{n+1}
R	S	
0	0	Q_n
0	1	1
1	0	0
1	1	Indeterminate

The logical operation of this device is such that when both the R and S inputs are "high" (logical "0"), the flip-flop will not change states. If the R input is "high" and the S input is "low," the device will go to the "1" state after the clock. Reversing the condition of the R and S inputs will reverse the output after the clock.

The condition where both the set and reset are "low" (logical "1") must be avoided. The output after clock for this condition is indeterminate. The Q output may go to a logical "one" or "zero." The logic equation for this flip-flop is:

$$Q_{n+1} = S^n + \bar{R}^n \cdot Q^n \qquad (4)$$

where

$R = S = 1$ is forbidden

(2). Circuit Analysis. To gain further insight into the logical operation of the RCTL flip-flop, it is necessary to analyze the circuit shown in Figure 1-39. The basic flip-flop consists of the transistors Q_2 and Q_5, with the appropriate R-C cross coupling. The steering inputs to the Q_2 side consist of Q_1, R_1, R_2 and $(CR)_1$. Capacitors C_1 and C_2 represent the clocking capacitors. Transistors Q_3 and Q_6 are the "preset" and "clear" transistors, respectively. The output complementary emitter-follower circuitry is the same as for the RCTL gate previously described.

Momentarily placing the "preset" input "high" will place the flip-flop into the "1" state, with Q_2 turned "on" and Q_5 turned "off." Now assume that the "reset" input has a "low" voltage ("1") and the "set" input is high ("0"). If the clock pulse signal is "low," the clock capacitor will be uncharged. When the clock pulse arrives (a positive-going pulse) the capacitor will charge on the leading edge of the pulse, through R_1 and $(CR)_1$. The polarity of this pulse will be negative on the side next to the cathode of the $(CR)_2$, with respect to the clock pulse input terminal. Now, when the clock pulse signal becomes a "low" voltage, the charge on the capacitor will forward-bias $(CR)_2$ and turn "off" Q_2. This will change the state of the flip-flop.

From the action of this circuit, several important points are disclosed:

- The clock line should remain "low" until clocking of the flip-flop is intended. (This will reduce noise susceptibility).
- The flip-flop will be clocked on the negative-going transition of the clock signal.
- If both the R and S inputs are "low," the clock pulse will try to switch both sides of the flip-flop "off."
- Since the clock capacitor is charged to the difference in potential between the clock signal and the steering input, it is possible to change the state of the flip-flop if the clock signal is exceptionally "high" with respect to the logical "0" state of the steering inputs, even if the steering inputs are moderately "high."

(3). Use of the Data Sheet

(a). General. The general philosophy expressed in the discussion of the data sheet used for the RCTL gate should also be applied to the data sheet of the flip-flop. That is, if the device is to be connected only within the device family (RCTL), the important characteristics are power dissipation, loading, and propagation delay. For a typical RCTL flip-flop data sheet, see Figure 1-40.

(b). Power. The figure for power dissipation is used to evaluate the system power requirements. The statements previously made in the discussion of the RCTL gate concerning the effect of temperature on the change in power, hold equally well for the flip-flop. It should be remembered that the flip-flop's power dissipation is continuous, whereas the gate power was specified for the "on" condition. Thus, duty-cycle correction does not apply in the case of the flip-flop power calculations.

(c). Loading. The data sheet specifies the maximum dc fan-out for both the collector output and the emitter-follower output. Since the opposite side of the flip-flop constitutes a load for the output, the fan-out will naturally be less than for the RCTL gate. If flip-flop loads are exceeded, not only will the devices that are acting as the load be starved, but the flip-flop transistors will not be properly saturated. This causes the flip-flop to be noise sensitive, and when the device is clocked, noise may cause illogical operation of the device.

TYPES SN 510 , SN 511

*SOLID CIRCUIT® DIFFUSED SILICON BISTABLE NETWORK

NETWORK CHARACTERISTICS

absolute maximum ratings

Supply Voltage . . . . . 8 Volts
Input Voltage (Set and Reset) . . . . . 8 Volts
Clock Pulse Voltage . . . . . 8 Volts (positive pulse)
Operating Ambient Temperature Range . . . . . − 55°C to +125°C
Storage Temperature . . . . . − 55°C to +125°C

network electrical characteristics	V_{CC} = 3V Min	Typ	Max	V_{CC} = 6V Min	Typ	Max	Units
Network Dissipation (T_A = 25°C; Fan-Out = 0)		2			7		mw
Loading							
Outputs Q & $\bar{Q}$ on SN 510 & SN 511							
DC Fan-Out (NOTE 1)			4			4	
Outputs Q* & $\bar{Q}$* (Emitter Follower — available only on SN 511)							
DC Fan-Out			20			20	
Input Voltage							
Typical Clock Pulse Voltage, (T_A 25°C) (NOTE 2)	0.35		1.7	0.40		2.7	Volts
(See curves on Page 3)							
CP Frequency = 100 KC							
t_f = 100 nsec							
PW = 500 nsec							
V_s ($\bar{S}$ or $\bar{R}$ steered input voltage) $V_{CC}/3$							
Preset Voltage, (T_A 125°C)	1.15			2.0			Volts
(T_A −55°C)	1.6			2.5			Volts
Set or Reset Voltage, (T_A 125°C)	1.15			2.0			Volts
(See curves on Page 3) (T_A −55°C)	1.6			2.5			Volts
Output Voltages							
Output Q & $\bar{Q}$ on SN 510 & SN 511							
OFF Level (T_A 125°C; N 0)	2.2			4.1			Volts
(T_A = 125°C; N = 4)	1.15			2.0			Volts
(T_A = −55°C; N = 4)	1.60			2.50			Volts
ON Level (T_A = 125°C)			0.22			0.30	Volts
(T_A = −55°C)			0.40			0.50	Volts
Outputs Q* & $\bar{Q}$* (Emitter Follower — available only on SN 511)							
OFF Level (T_A = 125°C; N = 20)	1.5			3.8			Volts
ON Level (T_A = 125°C)			0.22			0.30	Volts

NOTE 1: AC Fan-Out: When fanning-out into flip-flop clock pulse inputs (AC Load) the emitter-follower outputs on the SN 511 should be used for fan-outs above 5 or frequencies above 500 KC.

NOTE 2: The clock pulse must always be positive above the level of Pin 7. The values listed are ranges of typical clock pulse voltages.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SC07269(1-2)

Figure 1-40. Data Sheet for a Typical RCTL Flip-Flop (Types SN510, SN511) (Sheet 1 of 2)

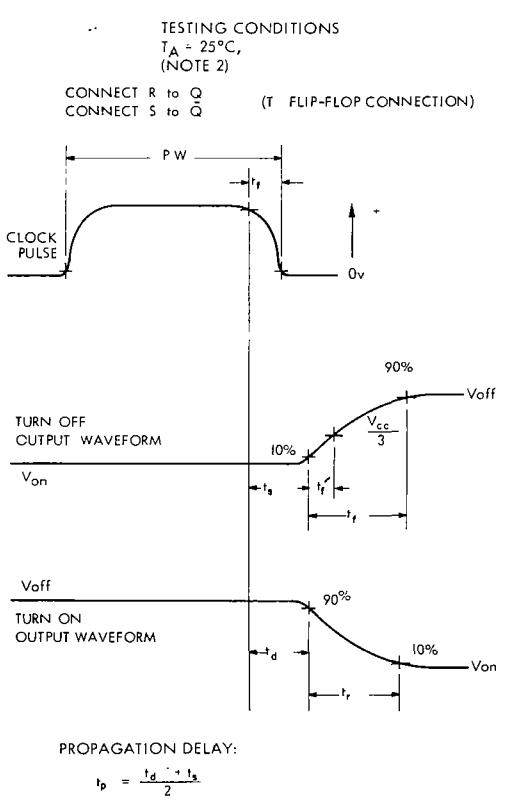
	V_{CC} = 3V			V_{CC} = 6V			
switching time (T_A = 25°C; N = 0) (NOTE 3) f = 40 KC, PW = 5 μsec, t_f = 100 nsec	Min	Typ	Max	Min	Typ	Max	Units
		Pulse Amp = 2v			Pulse Amp = 4v		
Delay Time (t_d)		300	500		170	300	nsec
Rise Time (t_r)		250	500		150	500	nsec
Storage Time (t_s)		120	200		120	200	nsec
Fall Time (t_f)		1.5	2.5		1.5	2.5	μsec
Time to Reach a Voltage to Set a Flip-Flop (t_f') (NOTE 4)		300	600		300	600	nsec
repetition rate (NOTE 5) Clock Pulse: Pulse amplitude (positive) = 2V, Pulse Width = 500 nsec, Fall Time = 100 nsec	0.8			1			mc

NOTE 3: There is no external load on the Flip-Flop outputs as specified. Triggering occurs at the negative edge of pulse as shown on waveforms.

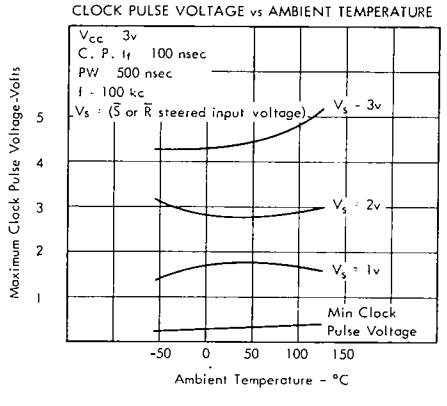
NOTE 4: This is the delay time necessary to steer a zero into either the R or S inputs of another flip-flop.

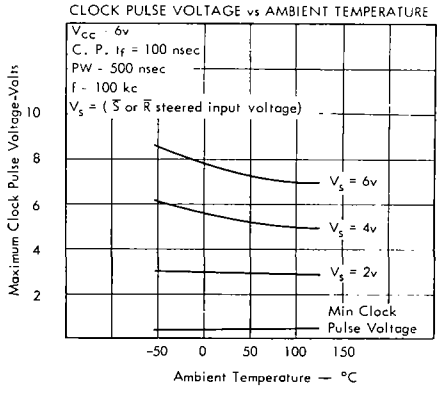
NOTE 5: This repetition rate is an indication of the maximum resolution of the network when N = 0. With loading, propagation delay curves indicate the time required to reach logic levels.

SWITCHING TIME VOLTAGE WAVEFORMS



TYPICAL CHARACTERISTICS





SC07270(2-2)

Figure 1-40. Data Sheet for a Typical RCTL Flip-Flop (Types SN510, SN511) (Sheet 2 of 2)

If the flip-flop is connected to discrete-component circuitry or other families of microcircuits, the other characteristics listed on the data sheet become important and useful. Careful attention should be paid to the maximum or minimum voltages specified for "preset," "clear," "set" and "reset."

(d). Inputs. The sensitive areas for the RCTL flip-flop lie in the "preset," "clear" and "clock" functions.

(1). Preset and Clear. The basic operation of the synchronous flip-flop is dependent upon the fact that the device will not change state until the occurrence of a clock pulse. The circuit will then remain in this state until the following clock pulse (depending upon the steering input). The "preset" or "clear" inputs will, however, change the state of the flip-flop at any time that these inputs exceed the dc noise margin. For this reason, these inputs should be as free of noise and decoding spikes as possible. If the inputs are not used, they should be connected to ground. More problems have arisen from the use of "preset" and "clear" inputs than from any other single function.

(2). Clock. The clock input to the RCTL flip-flop must meet several special requirements to insure best system operation. As previously mentioned, the clock pulse is a positive-going signal. The flip-flop triggers on the trailing edge of this pulse. The clock signal should be normally "low," with an "on" time of not less than 1 μs. Typically, the clock pulse should be less than 5 μs in duration. The fall time of the pulse should be less than 500 ns. The clock pulse should not occur when the "preset" or "clear" inputs are "high," and it should not occur until after the propagation of the "set" and "reset" inputs.

If at all possible, the clock-driver circuit should be used for driving the flip-flops. The RCTL clock driver provides all the necessary requirements for the flip-flop with respect to waveshape and amplitude, and is designed with a high a-c loading capacity. A typical data sheet for the clock driver is shown in Figure 1-41. This particular device is designated the SN517.

According to the data sheet, the device is capable of driving 20 flip-flop clock inputs. The input-output polarity is noninverting. To prevent the maximum amplitude of the output from exceeding the requirements of the flip-flop, terminal 7 must be tied to terminal 9.

c. Applications Summary

As a quick reference, the general application rules for the RCTL circuits are repeated here. For the RCTL gate circuits, the rules are:

TYPE SN517A
DIFFUSED SILICON "CLOCK DRIVER" NETWORK

absolute maximum ratings over operating free-air temperature range

Supply Voltage, V_{CC} (See Note 1)	+8 v
Input Voltage, V_{in} (See Notes 1 and 2)	V_{CC}
Operating Free-Air Temperature Range	−55°C to 125°C
Storage Temperature Range	−55°C to 125°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics

PARAMETER	TEST CONDITIONS	V_{CC} = 3 v			V_{CC} = 6 v			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Network Dissipation	Output Low, T_A = 25°C		7.5			33		mw
	Output High, T_A = 25°C		3.5			18		mw
Fan-In	T_A = −55°C to 125°C			1			1	
D-C Fan-Out	T_A = −55°C to 125°C			0			0	
A-C Fan-Out (See Note 3)	T_A = −55°C to 125°C			20			20	
Input Voltage That Will Ensure								
OFF Level	T_A = 125°C	1.15			2			v
	T_A = −55°C	1.6			2.5			v
ON Level	T_A = 125°C			0.22			0.3	v
	T_A = −55°C			0.4			0.5	v
Output Voltage								
OFF Level	T_A = 125°C, V_{out} not clamped, Fan-Out = 0	2.5			5			v
	T_A = 125°C, V_{out} clamped, Fan-Out = 0	0.95		1.25	1.4		2.1	v
	T_A = −55°C, V_{out} clamped, Fan-Out = 0	1.25		1.65	1.7		2.6	v
ON Level	T_A = 125°C			0.22			0.3	v
	T_A = −55°C			0.22			0.3	v

NOTE 3: When driving clock inputs of SN510A, SN511A, SN5101, or SN5111, pin (9) of the SN517A should be grounded (clamped) to limit the output voltage. When driving SN5112 or SN5113 clock inputs, output voltage should not be clamped and pin (9) should be connected to V_{CC}.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SC07271(1-2)

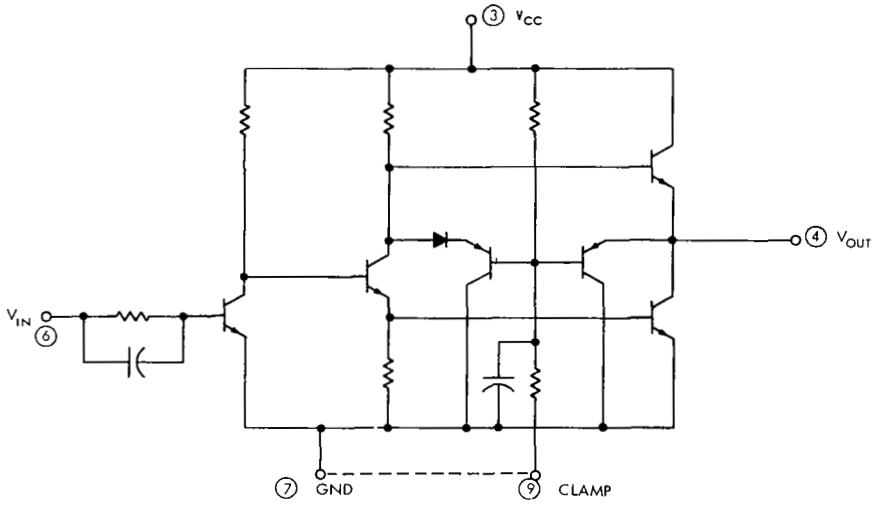
Figure 1-41. A Typical Data Sheet for an RCTL Clock Driver (Type SN517A) (Sheet 1 of 2)

switching characteristics, $T_A = 25°C$, a-c fan-out = 20, V_{out} not clamped

PARAMETER	TEST CONDITIONS	$V_{CC} = 3$ v, $V_{in} = 2$ v		$V_{CC} = 6$ v, $V_{in} = 4$ v		UNIT
		TYP	MAX	TYP	MAX	
t_d Delay Time	*Input signal:* $t_r = t_f = 100$ nsec,	300	500	180	320	nsec
t_r Rise Time	$t_p = 2$ μsec, f = 100 kc,	300	500	300	500	nsec
t_s Storage Time	See Figures 1 and 2	200	300	140	240	nsec
t_f Fall Time		0.6	1.4	0.8	1.6	μsec

schematic

CIRCUIT DIAGRAM



NOTES: 1. Dotted connection shows clamped condition.
2. Pins ①, ②, ⑤, and ⑩ — no internal connection.
3. Do not make external connection at pin ⑧.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 1-41. A Typical Data Sheet for an RCTL Clock Driver (Type SN517A) (Sheet 2 of 2)

- Unused inputs should be connected to circuit ground.
- The voltage level of the input signals should not be forced below ground nor exceed the V_{CC} voltage.
- The fan-out capability should not be exceeded.

The general application rules for the RCTL flip-flops are:

- The steering input of R = S = 1 is forbidden.
- The clock should be a positive-going pulse, with the negative transition being used to trigger the flip-flop.
- The clock signal should be normally "low." The pulse should have a minimum 1-μs "on" time.
- In the "high" condition, the maximum voltage of the clock pulse should be limited so that the excess over the value of the "set" or "reset" inputs does not exceed the amount specified in the data sheets.
- The "preset" and "clear" inputs should be "clean"—no spikes or other noise.
- The "preset" and "clear" inputs should not be "high" at the same time as the clock input.
- The fan-out capabilities should not be exceeded.

3. DTL Type Circuits

a. Gate

(1). Circuit Description. A basic DTL gating element is shown in Figure 1-42. This is a 3-input NAND/NOR gate. The actual microcircuit usually contains several gates within the same die and package. The input diodes D_1 through D_3 and resistors R_1 and R_2 form the AND function of the circuit. The output is taken off the collector of the inverting transistor, Q_2, which provides the NOT function. Transistor Q_1 provides additional drive current for the output transistor, Q_2.

(2). Circuit Analysis. The logic equations for the circuit are given in Figure 1-43. If any one or more of the inputs is at a "low" voltage level, the respective input diode will be conducting in the forward direction. Current will be flowing through R_1 and R_2 and out from the input and into the driving source. The voltage at the base of Q_1 is low enough to keep transistor Q_1 cut "off"; thus, transistor Q_2 will be in the "off" state. This provides a "high" voltage at the output.

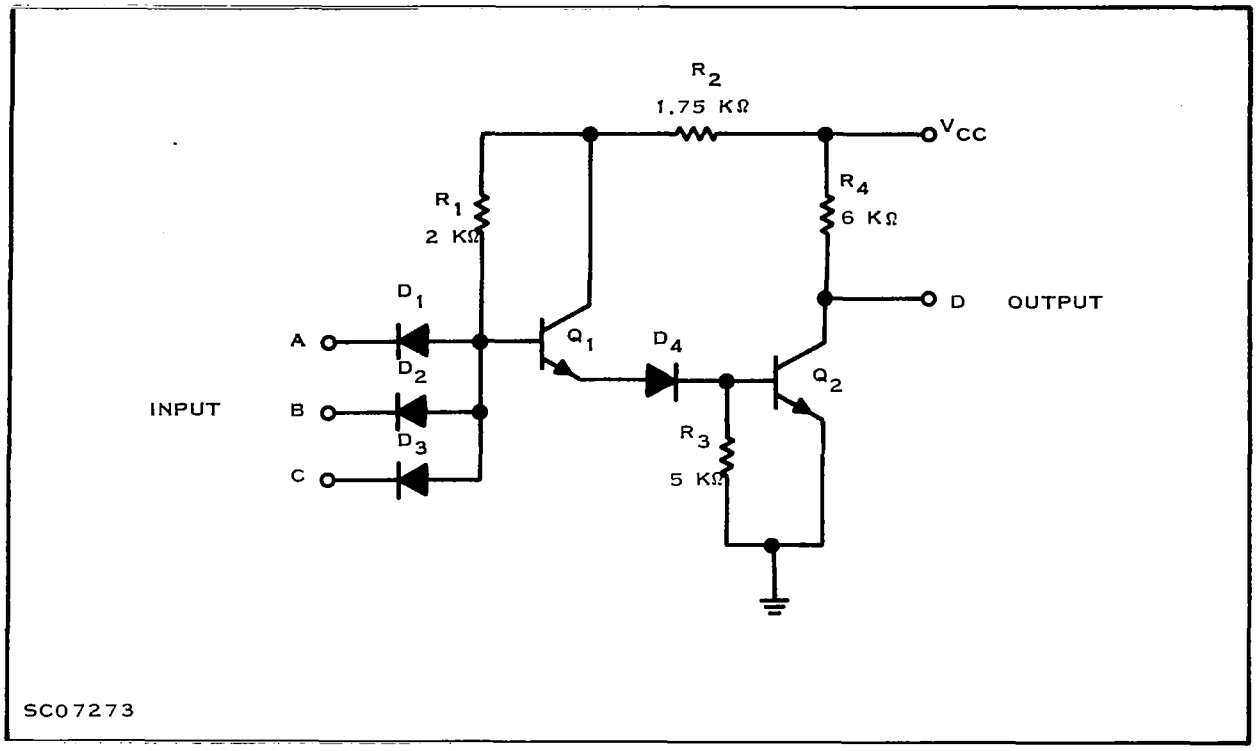


Figure 1-42. Schematic of a Basic DTL Gate

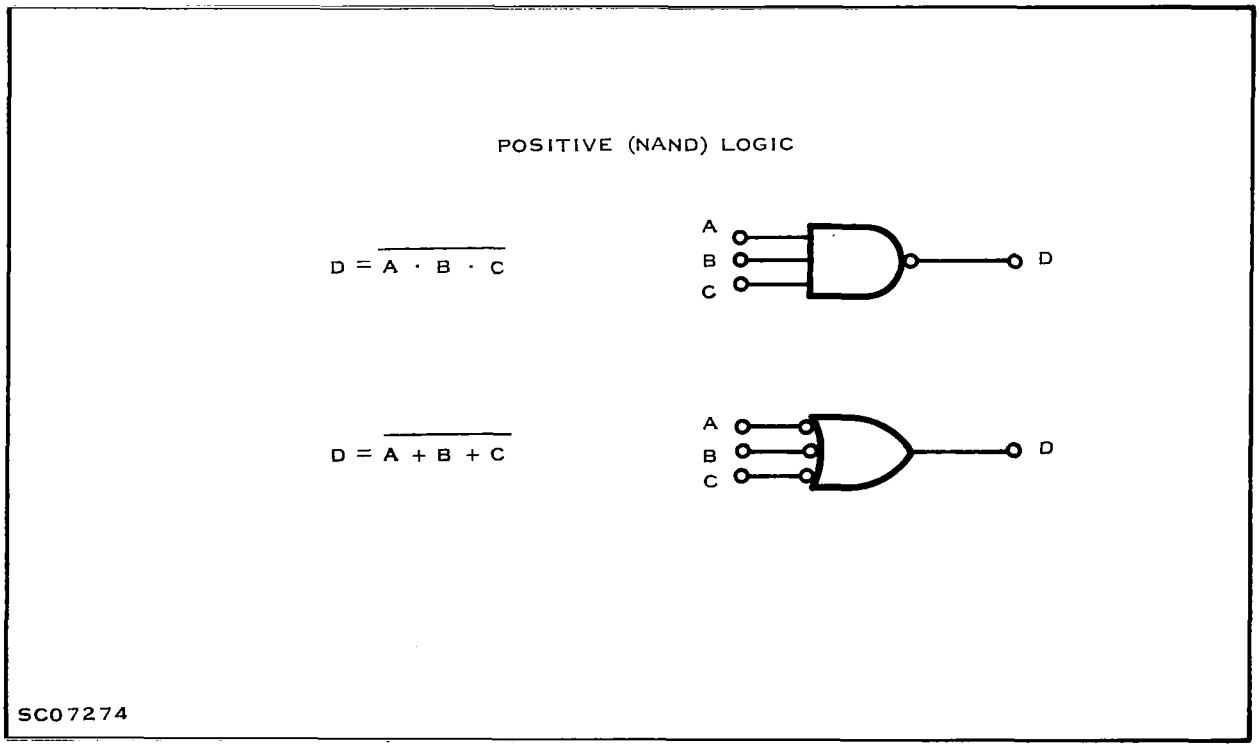


Figure 1-43. Logic Diagram for DTL Gate

When all of the inputs are at a "high" voltage level, transistor Q_1 is turned "on" by the bias resistors R_1 and R_2. Transistor Q_1 turns "on" transistor Q_2, bringing the output to a "low" voltage level.

(3). Use of the Data Sheet

(a). General. Using the data sheet (Figure 1-44) for the SN15930 microcircuit, the electrical characteristics of the DTL gate will be discussed. The SN15930 is a dual 4-input NAND/NOR gate with expander nodes on the input for increasing the fan-in capabilities.

(b). Power. The recommended operating conditions are: supply-voltage range of 4.5 to 5.5 V, and maximum fan-out of 8 from each output. Even though the circuit has a maximum supply of 8 V with respect to ground and would operate at other voltages, the circuits have been characterized for operation between 4.5 V and 5.5 V and should be operated within this range. Each electrical characteristic is tested at the worst-case supply voltage. The fan-out of 8 means that 8 identical inputs can be driven from one output.

(c). Output Voltages

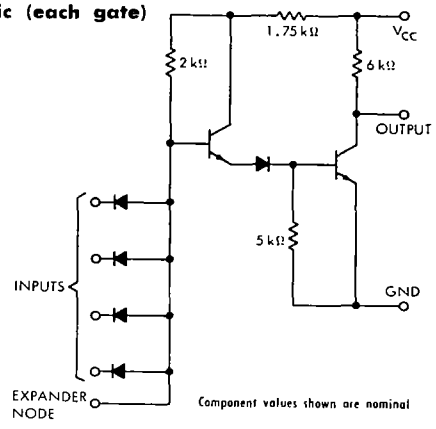
(1). General. The first two parameters listed are the logical "0" and logical "1" voltage levels at the output. Even though the circuits are tested at different temperatures, only the worst-case test will be discussed, since it is the one that must be considered in system design.

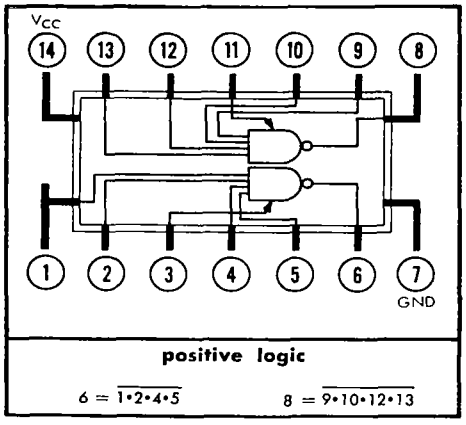
(2). "On" Level. The output "on" level, $V_{out(0)}$, worst-case occurs at +125°C. All of the inputs (except the expander node) are connected to 1.7 V. Maximum fan-out is connected to the output indicated by the 10.8 mA sink current. The output voltage is tested for a maximum voltage of 0.45 V; the circuit is rejected if the voltage is greater.

(3). "Off" Level. The output "off" level, $V_{out(1)}$, worst-case occurs at 25°C and 125°C. Each input, one at a time, is connected to a 0.5 V supply (125°C) and the output is tested for a minimum voltage of 2.5 V. Therefore, for the SN15930, eight "off" level tests are performed for each test temperature. Again, the outputs are loaded with maximum fan-out. If the output voltage is lower than the minimum limit, the circuit will be rejected.

(4). Testing the Level. One important aspect used in testing the voltage level is the difference between the voltage test level applied to the inputs, and the test limit. For example, the "off" voltage is tested for a minimum of 2.5 V, but for the output "on" level test, an "off" level voltage of 1.7 V is applied to the inputs. This difference of 0.8 V insures the logic operation for system variations

schematic (each gate)





recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum Fan-Out From Each Output 8

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = 4.5 V, V_{in} = 1.9 V, I_{sink} = 12 mA, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 2.1 V, I_{sink} = 11.4 mA, T_A = −55°C		0.4	V
			V_{CC} = 4.5 V, V_{in} = 1.7 V, I_{sink} = 10.8 mA, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level)	2	V_{CC} = 4.5 V, V_{in} = 1.1 V, I_{load} = −0.12 mA, T_A = 25°C	2.6		V
			V_{CC} = 4.5 V, V_{in} = 1.4 V, I_{load} = −0.12 mA, T_A = −55°C	2.5		V
			V_{CC} = 4.5 V, V_{in} = 0.8 V, I_{load} = −0.12 mA, T_A = 125°C	2.5		V

† Expander nodes are open unless otherwise noted.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SC07275(1-2)

Figure 1-44. Data Sheet for a DTL Gate (Type SN15930) Dual Four-Input NAND/NOR Gate (Sheet 1 of 2)

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(1)}$	Logical 1 output voltage (off level) with low voltage at expander input node, $V_{in\,x}$	3	V_{CC} = 4.5 V, $V_{in\,x}$ = 1.8 V, I_{load} = −0.12 mA, T_A = 25°C	2.6		V
$I_{in(1)}$	Logical 1 level input current	4	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level input current	5	V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 25°C and −55°C		−1.6	mA
			V_{CC} = 5.5 V, V_{in} = 0, V_R = 4 V, T_A = 125°C		−1.5	mA
$I_{out(1)}$	Output reverse current (off level)	6	V_{CC} = V_{out} = 4.5 V, T_A = 25°C		50	μA
I_{OS}	Short-circuit output current	7	V_{CC} = 5.5 V, V_{out} = 0, T_A = 25°C	−0.6	−1.34	mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = −55°C		−1.34	mA
			V_{CC} = 5.5 V, V_{out} = 0, T_A = 125°C		−1.3	mA
$I_{CC(0)}$	Logical 0 level supply current (both gates)	8	V_{CC} = 5 V, T_A = 25°C		6.5	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC} (both gates)	9	V_{CC} = 8 V, T_A = 25°C		5.5	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$t_{pd(0)}$	Propogation delay time to logical 0 level	51	R_1 = 400 Ω, C_L = 50 pF	10	30	ns
$t_{pd(1)}$	Propogation delay time to logical 1 level		R_1 = 3.9 kΩ, C_L = 30 pF	25	80	ns

† Expander nodes are open unless otherwise noted.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SC07276(2-2)

Figure 1-44. Data Sheet for a DTL Gate (Type SN15930) Dual Four-Input NAND/NOR Gate (Sheet 2 of 2)

and guarantees an 0.8-V noise immunity. The same is true for the "on" level test, where an "on" level of 0.8 V is applied to the input, and the test limit is 0.45 V. However, only 350 mV difference between input and test limit is used during this test. Additional tests are performed on the expander inputs.

(d). Input Currents. The input currents are tested for each input at the logical "1" and logical "0" levels. The logical "1" level input current, $I_{in(1)}$, is tested with V_{CC} = 5.5 V and input voltage V_{in} = 4 V. The high test-voltages insure worst-case conditions. Actually, this is a measurement of the input-diode leakage current. The worst-case limit is 5 uA, and for a fan-out of 8, the output must be capable of supplying 40 uA of current. This is well below the test of 0.12 mA used for the "off" voltage test.

The logical "0" level input current, $I_{in(0)}$, is tested with V_{CC} = 5.5 V, and V_{in} = 0 V. The maximum limit for this test is 1.6 mA. This indicates that for a fan-out of 8, the output must sink 12.8 mA of current. A current of 12.8 mA is somewhat higher than the test conditions for the "on" level voltage test. Since this is a worst-case condition, it probably could never be duplicated in system design. However, this does seem to indicate that for a high reliability application, the maximum fan-out should be derated.

The previously described tests are used to provide the correct dc interface parameters for a microcircuit. Other tests are performed to insure the device will operate within the intended application. A short-circuit output current test insures that the device will not be destroyed if the output is shorted to ground.

The supply current is tested to give an indication of the maximum amount of supply power needed within a system.

(e). Propagation Delay. The switching characteristics are measured at 25°C. The propagation delay times are a function of temperature, fan-out, load capacitance, and V_{CC}. It would be impossible to use all of these variables to test the switching times. Instead, the switching times are tested under worst-case conditions (except for temperature). The maximum limits are considered adequate under normal system conditions. To insure a more reliable system, the circuits should not be operated close to their maximum limits.

b. Flip-Flop

(1). Circuit Description. A data sheet for the DTL flip-flop circuit is shown in Figure 1-45. The 948 master-slave flip-flop has AND gate inputs to its master section, which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and the slave sections. The sequence of operation follows this order: as the clock pulse starts

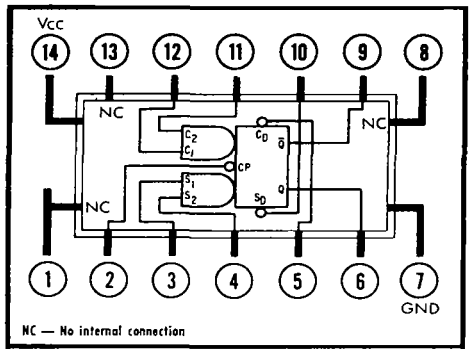
logic

TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

NOTES. 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0.
5. For operation in the J-K mode connect S_2 to $\overline{Q}$ and C_2 to Q.



positive logic

Low input to S_D sets Q to logical 1

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V
Maximum Fan-Out From Each Ouput 9

electrical characteristics

PARAMETER		TEST FIGURE	TEST CONDITIONS			MIN	MAX	UNIT
$V_{out(0)}$	Logical 0 output voltage (on level) at Q or $\overline{Q}$	27 and 28	V_{CC} = 4.5 V, V_3 = 4.5 V,	V_1 = 1.1 V, I_{sink} = 13.6 mA,	V_2 = 1.9 V, T_A = 25°C		0.4	V
			V_{CC} = 4.5 V, V_3 = 4.5 V,	V_1 = 1.4 V, I_{sink} = 13 mA,	V_2 = 2.1 V, T_A = −55°C		0.4	V
			V_{CC} = 4.5 V, V_3 = 4.5 V,	V_1 = 0.8 V, I_{sink} = 12.3 mA,	V_2 = 1.7 V, T_A = 125°C		0.45	V
$V_{out(1)}$	Logical 1 output voltage (off level) at Q or $\overline{Q}$	12	V_{CC} = 4.5 V, I_{load} = −0.12 mA,	V_1 = 4.5 V, T_A = 25°C	V_2 = 1.1 V,	2.6		V
			V_{CC} = 4.5 V, I_{load} = −0.12 mA,	V_1 = 4.5 V, T_A = −55°C	V_2 = 1.4 V,	2.5		V
			V_{CC} = 4.5 V, I_{load} = −0.12 mA,	V_1 = 4.5 V, T_A = 125°C	V_2 = 0.8 V,	2.5		V
$I_{CP(0)}$	Logical 0 level clock-input forward current	29	V_{CC} = 5.5 V, T_A = 25°C	V_{in} = 1.1 V,	V_{CP} = 0,		−2.56	mA
			V_{CC} = 5.5 V, T_A = −55°C	V_{in} = 1.4 V,	V_{CP} = 0,		−2.56	mA
			V_{CC} = 5.5 V, T_A = 125°C	V_{in} = 0.8 V,	V_{CP} = 0,		−2.2	mA
$I_{CP(1)}$	Logical 1 level clock-input reverse current	30	V_{CC} = 4 V, T_A = 25°C and −55°C	V_{CP} = 4 V,			10	μA
			V_{CC} = 4 V,	V_{CP} = 4 V,	T_A = 125°C		20	μA

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SC07277(1-3)

Figure 1-45. Schematic of a DTL Flip-Flop (Type SN15948) (Sheet 1 of 3)

electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level synchronous-input current	31	V_{CC} = 5.5 V, V_{in} = 0, V_1 = 4 V, V_{CP} = 4 V, T_A = 25°C and −55°C		−1.07	mA
			V_{CC} = 5.5 V, V_{in} = 0, V_1 = 4 V, V_{CP} = 4 V, T_A = 125°C		−1	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	32	V_{CC} = 5.5 V, V_{in} = 4 V, V_1 = 5.5 V, T_A = 25°C and −55°C		2	μA
			V_{CC} = 5.5 V, V_{in} = 4 V, V_1 = 5.5 V, T_A = 125°C		5	μA
$I_{in(0)}$	Logical 0 level asynchronous-input current	33	V_{CC} = 5.5 V, V_{in} = 0, T_A = 25°C and −55°C		−2.4	mA
			V_{CC} = 5.5 V, V_{in} = 0, T_A = 125°C		−2.1	mA
I_{OS}	Short-circuit output current	18	V_{CC} = 5.5 V, V_{in} = 5.5 V, V_{out} = 0, T_A = 25°C and −55°C	−2.1	−3.96	mA
			V_{CC} = 5.5 V, V_{in} = 5.5 V, V_{out} = 0, T_A = 125°C		−3.54	mA
$I_{CC(0)}$	Logical 0 level supply current	19	V_{CC} = 5 V, T_A = 25°C		16.2	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum V_{CC}	20	V_{CC} = 8 V, T_A = 25°C		16	mA

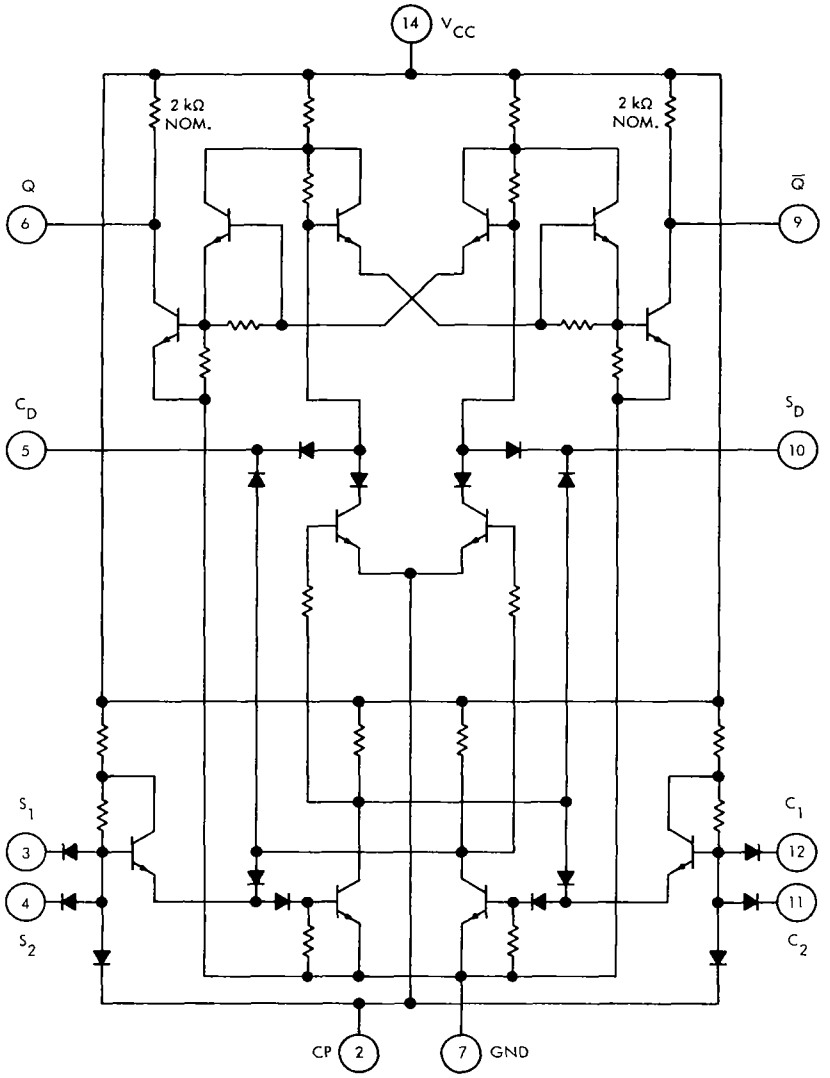
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	R_1 = 330 Ω, C_L = 50 pF		65	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		R_1 = 2 kΩ, C_L = 30 pF		75	ns

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 1-45. Schematic of a DTL Flip-Flop (Type SN15948) (Sheet 2 of 3)

schematic



NOTE: Pins (1), (8) and (13)—no internal connection.

SC07279(3-3)

Figure 1-45. Schematic of a DTL Flip-Flop (Type SN15948) (Sheet 3 of 3)

"high," the slave portion is isolated from the master. When the pulse reaches a certain height, information from the AND gate inputs are entered into the master portion. As the clock pulse starts down, the AND gate inputs are disabled, and, as the pulse reaches a "low" level, the information is transferred from the master to the slave.

As shown by the truth tables of Figure 1-45, the 948 flip-flop can be operated in either the R-S or J-K mode. A J-K flip-flop toggles whenever its inputs are both at the logical "1" ("high" voltage) level. Whereas, if both inputs are "high" on an R-S flip-flop, the output is indeterminate. This indeterminate state is undesirable in many system applications. The J-K operation is accomplished by connecting the Q output to the C_2 input and the $\overline{Q}$ output to the S_2 input. The J-K flip-flop is an R-S flip-flop that has its input gating activated by its outputs, which causes the flip-flop to toggle when C_1 and S_1 are both at the logical "1" level.

(2). Electrical Tests. The electrical characteristic for the flip-flop is presented in Figure 1-45. Much more testing is necessary for the flip-flop than for the basic gate. There must be sufficient testing to insure that the circuit performs according to the truth tables. To insure compatibility with the gating elements, the flip-flop is tested to the same logical "1" and logical "0" voltage levels.

Note that the input current to the clock is approximately twice that of the basic gate. Therefore, when using a basic gate to drive the clock, the clock input must be considered as a fan-out of two. Also, the logical "0" level input current for the J-K flip-flop (asynchronous-input current) is higher than the input current for the same tests of the basic gate. As pointed out in the earlier discussion of digital circuit parameters, it is necessary to define the fan-out in terms of the actual current requirement.

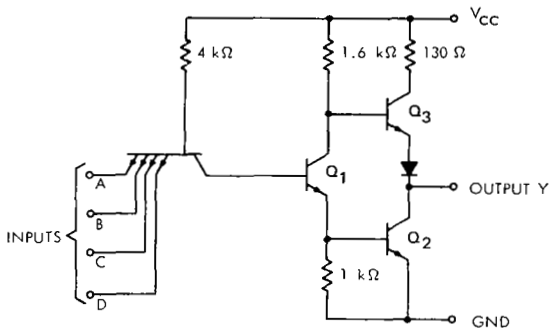
4. TTL Type Circuits

a. Gate

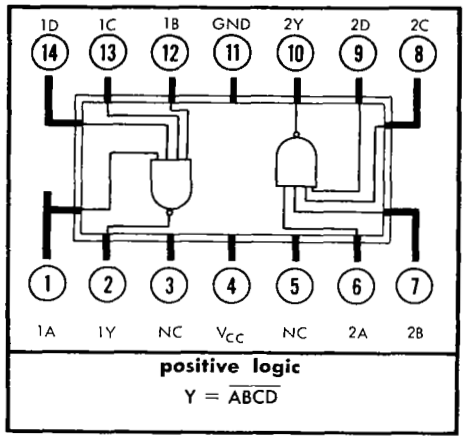
(1). Circuit Analysis. The operation of the basic TTL gate is very similar to the DTL gate discussed previously. The only differences are the use of the multi-emitter input transistor instead of diodes, and a stacked transistor on the output to provide better drive capabilities.

The data sheets for a TTL gate (SN5420) are shown in Figure 1-46. The operation of the circuit is such that when all four inputs are "high," the output is "low." If one of the inputs is "low," the output will be "high." When all inputs are "high," the current will be diverted from the emitters of the multiple-emitter transistor to the collector. This turns "on" transistor Q_1, which turns "on" transistor Q_2; therefore, the output is "low." When one of the emitters of the multiple-emitter transistor is "low," the current from the base is diverted through the emitter;

schematic (each gate)



Component values shown are nominal.



recommended operating conditions

Supply Voltage V_{CC}	4.5 V to 5.5 V
Fan-Out From Each Output, N	1 to 10

electrical characteristics, $T_A = -55°C$ to 125°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.5 V,	$V_{out(0)} \leq$ 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.5 V,	$V_{out(1)} \geq$ 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.5 V, I_{load} = −400 μA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.5 V, I_{sink} = 16 mA	V_{in} = 2 V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.5 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.5 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.5 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.5 V		−20		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		3		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_L = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_L = 15 pF		18	29	ns

†Not more than one output should be shorted at a time.

‡These typical values are at V_{CC} = 5 V.

SC07284

Figure 1-46. Data Sheet for a TTL Gate (Type SN5420)

thus, the base of Q_1 is starved for current. Therefore, the base of Q_3 is held "high," which turns "on" transistor Q_3, causing the output to go "high." The diode in the emitter of Q_3 provides protection from surge current when both Q_3 and Q_2 are "on" during transition periods. When transistor Q_1 is "on," the voltage drop across the 1.6 kΩ resistor does not bring the collector of Q_1 as "low" as the collector of Q_2. The diode in series with the emitter of Q_3 allows the base of Q_3 to be slightly positive with respect to the output without turning the transistor "on." An 0.8-V input at any of the gate inputs will cause the output of a gate to be 2.4 V or greater, with 10 loads tied to the output. With all inputs of a gate at 2 V, the output voltage will be no greater than 0.4 V for a load equal to 10 gates. This means that while an input will operate with a voltage as great as 0.8 V, it will never be required to see a voltage greater than 0.4 V, thereby providing a 0.4-V noise margin. Also, the output will be 0.4 V or less when the inputs are at 2.0 V, while the gate will never present a voltage of less than 2.4 V at any of the inputs. This, therefore, provides a noise margin of 0.4 V on the inputs that are "high."

(2). Electrical Tests. The electrical testing of the TTL circuits is performed under worst-case conditions, as with the DTL devices. The main difference is that for TTL circuits, one limit is given for the full temperature range. The data sheet provides only limited information on temperature variations of parameters, but this makes system design somewhat easier in that worst-case limits are given automatically.

b. Flip-Flop

(1). General. A detailed discussion of the logic operation of three basic types of available TTL flip-flops, the SN5470, SN5472 and SN5473 will now be presented. The SN5472 and the SN5473 are the same circuit except that the SN5473 is a dual flip-flop with only one J and one K input. The preset input is not available. Since the SN5473 is a simplified version of the SN5472, the SN5473 will be discussed first.

(2). Type SN5473

(a). Circuit Description. The SN5473 flip-flop is a master slave type, which means that the data present at the inputs are first stored in a master section of the flip-flop and then transferred to the slave or output section. A logic diagram of the SN5473 is shown in Figure 1-47. The master portion of the flip-flop consists of gates A, A', B, and B'. The slave portion consists of gates E and E'. The clear function is provided by gate C. Connection of the master and slave sections is accomplished by use of transistors D and D'. The clock input signal to the flip-flop controls the operation of the master and slave sections. Three basic logic symbols are used in the logic diagram. The first symbol is for gates A, A', and C, and it

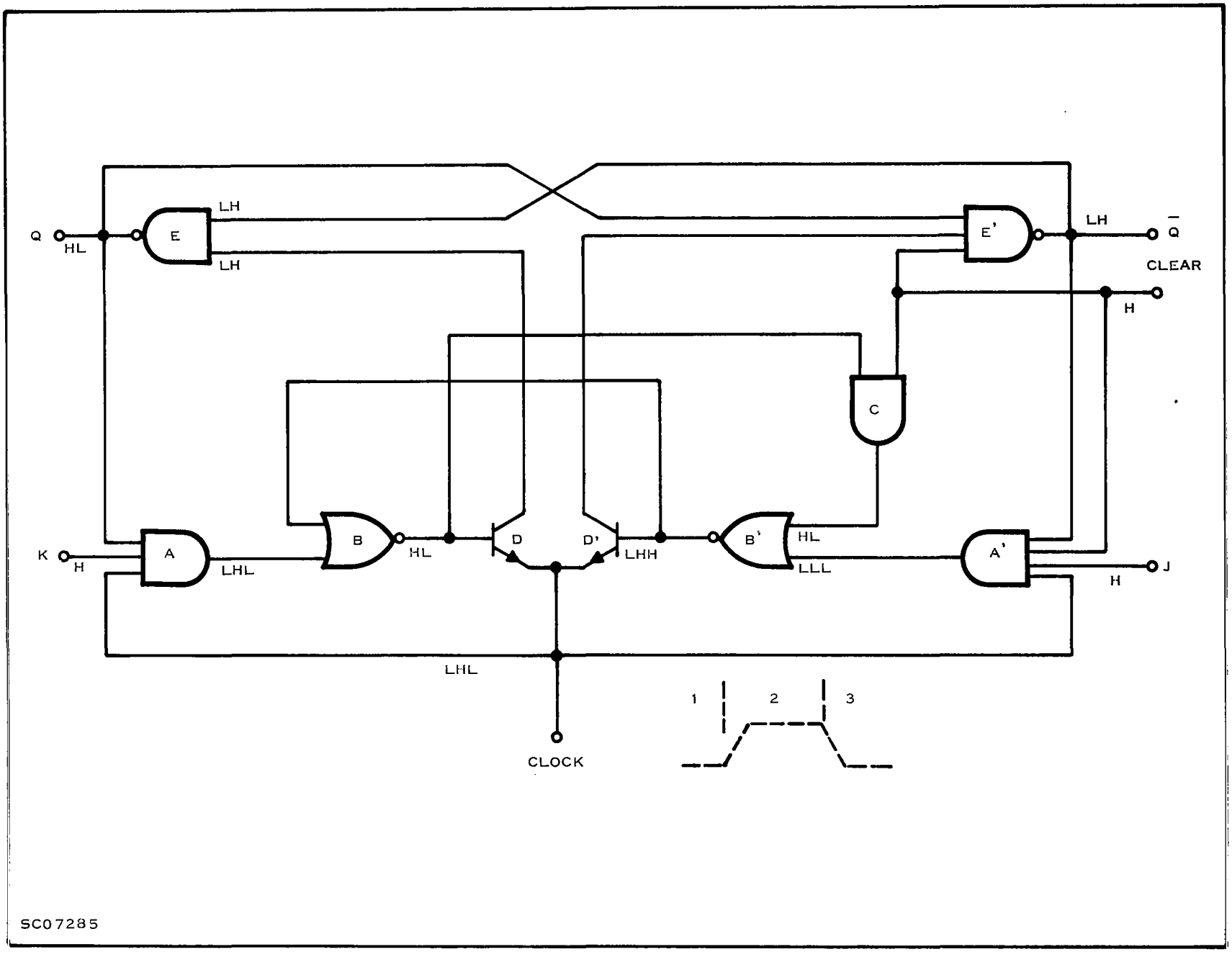


Figure 1-47. Logic Diagram for a TTL Flip-Flop with J-K High (Type SN5473)

represents a gate whose output is at a "high" potential only if all of its inputs are at a "high" potential. The second symbol is used for gates B and B' and represents a gate whose output is at a "low" potential if either of its inputs is "high." The third symbol is for gates E and E' and represents a gate whose output is "high" if any of the inputs are "low."

(b). Circuit Analysis. To discuss the operation of the circuit, assume that the Q output, "clear" input, and the J and K inputs are "high." During Region No. 1 of the clock period the clock input is "low," and as a result, gates A and A' are both "low." Since the Q output is "high," the base of transistor D also must be "high"; since both inputs of gate C are "high," the output of gate C is "high." A "high" input to gate B' causes the output to be "low"; therefore, both inputs to gate B are "low," thus forcing its output "high." During Region No. 2 of the clock period, the clock line goes "high," enabling gates A and A' to be controlled by the other inputs to these gates. In the assumed conditions for this analysis, the other inputs to gate A are "high," forcing the output "high." Since the $\bar{Q}$ output of the flip-flop is "low," the output of gate A' will remain "low" during Region No. 2. A "high" voltage at the input of gate B causes the outputs of gate B and gate C to go "low." The output of B' will change to a "high" state because both inputs are now "low." The "high" output of gate B' holds the output of gate B "low." A "high" at the output of B' will tend to cause transistor D' to turn "on," but the emitter of D' is held "high" by the clock, therefore, the transistor will not turn "on." This describes how the master portion of the flip-flop is controlled while the slave portion is not affected.

During Region No. 3, the clock line returns to the "low" state, thereby enabling transistor D' to turn "on." Transistor D will remain "off" because the base is at the same potential as the emitter. When transistor D' turns "on," one of the inputs to E' is forced "low," causing E' to change from a "low" to a "high" state. The "high" state of E' is fed back to an input of gate E, which causes the output of E to change from a "high" to a "low" state. The latching action of gates E and E' will keep them in their present state. Transistor D' will aid in keeping E' "high." Thus, during Region No. 3, the slave portion of the flip-flop is allowed to change states. If at some time before the slave portion of the flip-flop is allowed to change states, the "clear" input goes "low," E' will be forced to a "high" state. This causes the slave portion to change states immediately. In addition, the "clear" input's change to a "low" will cause the output of gate C to remain "low," regardless of the state of gate B. Gate C will remain "low" as long as the "clear" input is "low," therefore, both inputs to gate B' will remain "low" for this same period of time. Output B' is therefore "high," causing B output to go "low." These actions are independent of gate A. If the "clear" cycle begins before the clock pulse, transistor D' is turned "on" and transistor D is turned "off." If the clock pulse occurs before the "clear" pulse is removed, both transistors (D and D') will be turned "off." However, this does not affect the slave portion of the flip-flop. If the "clear" pulse is then

removed, the slave portion of the flip-flop does not change and the master portion holds the state set by the "clear signal. When the trailing-edge of the clock pulse occurs, transistor D' is again turned "on" to aid in keeping gate E' "high."

If the $\overline{Q}$ output of the flip-flop had been "high" when the "clear" pulse occurred, there would have been no change in the state of the master or slave sections,because a "clear" pulse at C input would have had no effect, since the other input to C was already "low," forcing the output low. At gate E', a "low" input would have been redundant because transistor D' and the Q output of the flip-flop would have acted to keep gate E' "high."

As a second example, consider the case where the Q output and K input are "low," and the J input and "clear" input are both high. (See Figure 1-48.) These conditions will cause the Q output to go "high" at the next clock pulse. During Region No. 1 of the clock period, both gates A and A' are disabled by the "low" signal from the clock. Transistor D' is turned "on" by the latching action of gates B and C. During Region No. 2 of the clock period, the clock input changes to a "high," which causes gate A' to go "high," while gate A remains "low." A "high" output from gate A' causes B' to go "low," and B to go "high" and to feed back through gate C to keep the input of B' "high" and B' output "low." This latching action causes transistor D to be biased "on" when the clock signal goes "low." The trailing edge of the clock pulse causes the slave section to change states such that the Q output is "high" and the $\overline{Q}$ output is "low."

If the "clear" input goes "low" during Region No. 2 of the clock pulse, the slave portion of the flip-flop does not change, since the $\overline{Q}$ output is already "high." However, the output of gate C is forced "low." At the same time, A' goes "low" because one of its inputs, "clear," has changed to the "low" state. With both inputs to B' "low," the output goes "high," forcing the output of B "low." This causes the base of transistor D' to be biased "high," and D to be biased "low." When the clock pulse enters Region No. 3, transistor D' is turned "on," holding the $\overline{Q}$ output "high" and the output of A' "low." When the "clear" line returns to the "high" state, no change is made in the state of gates C or A'. As a result, the $\overline{Q}$ output of the flip-flop remains "high."

(3). Type SN5472

(a). Circuit Description. The previous discussion demonstrated the logic operation of the SN5473 flip-flop for changes in the J, K, and "clear" inputs. It has been shown that the operation of the "clear" input is independent of the clock and of the J and K inputs. For the SN5472 flip-flop, the operation is the same, with the additional ability to preset as well as clear the flip-flop. As shown in Figure 1-49, the preset operation is the same as the "clear" function except that the preset

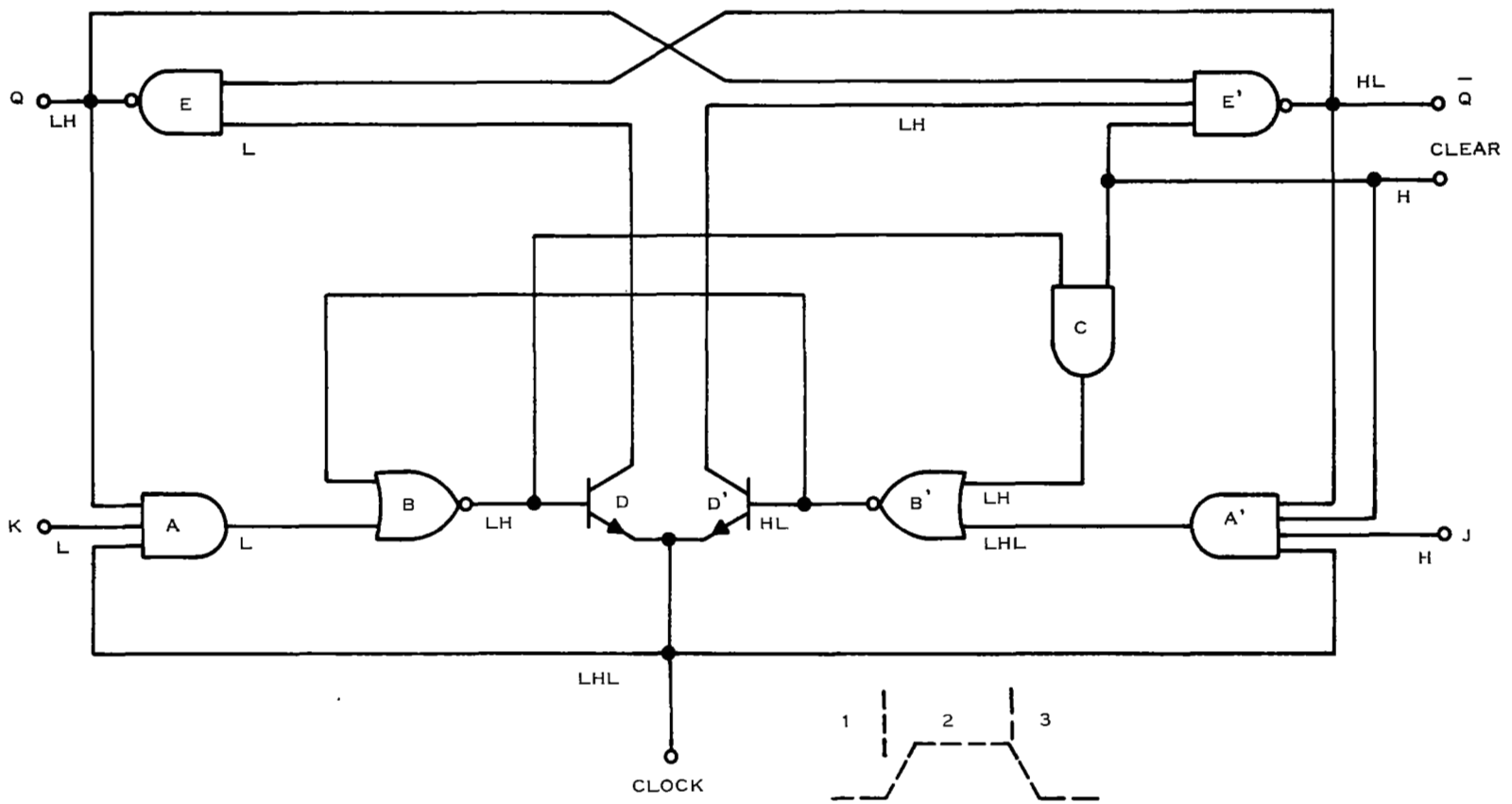


Figure 1-48. Logic Diagram for a TTL Flip-Flop with J-K High (Type SN5473)

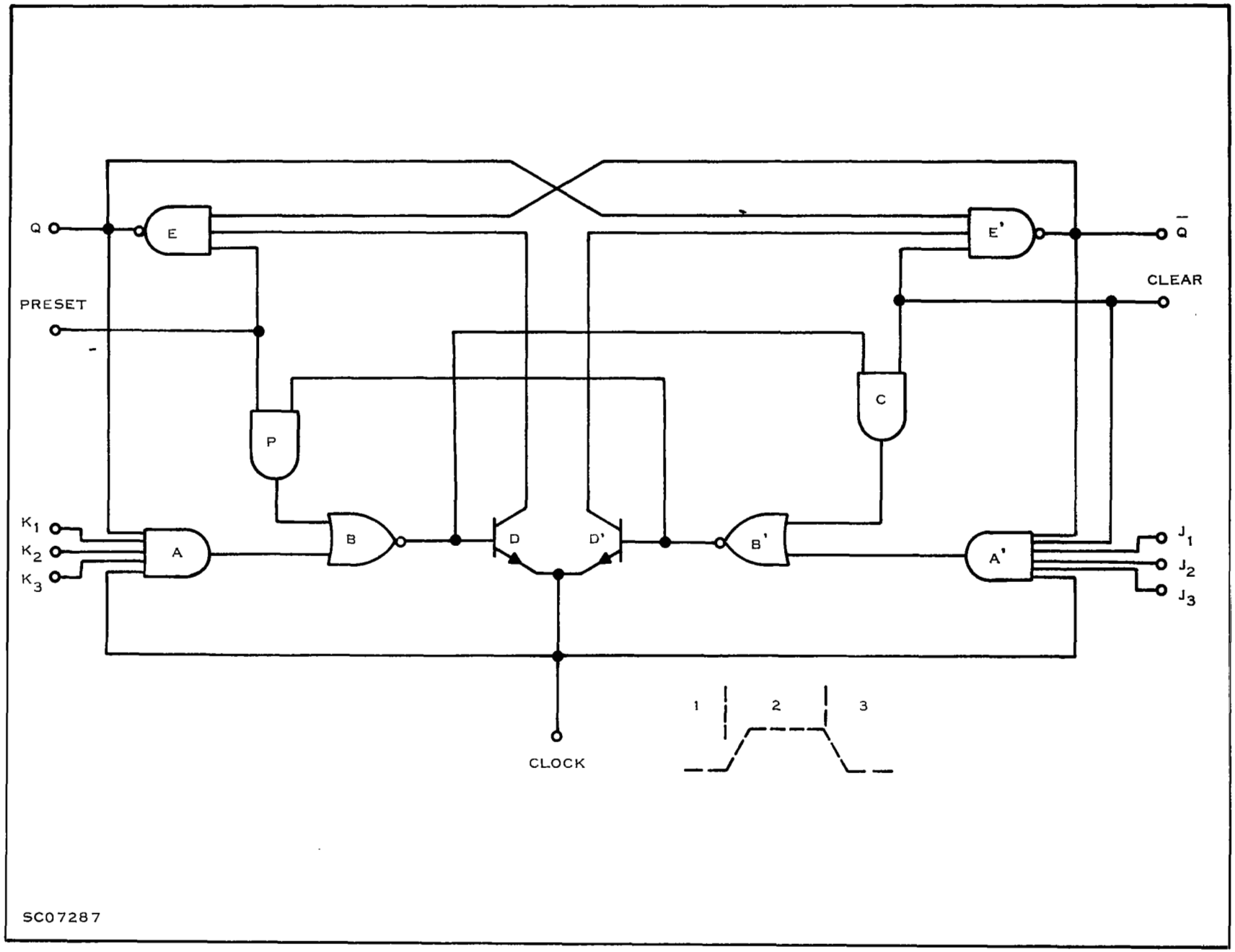


Figure 1-49 Logic Diagram for a TTL Flip-Flop (Type SN5472)

input causes the Q output to go "high." Also, in the SN5472 flip-flop, three K and three J inputs are provided. For the flip-flop to toggle, the three K inputs and the three J inputs must be "high." For the Q output to be "high" the three J inputs must be "high," and for the $\overline{Q}$ output to be "high" the three K inputs must be "high." A "preset and clear" pulse must not be preset at the same time because this would tend to cause both Q and $\overline{Q}$ outputs to go "high," resulting in a race condition, with the final state of the flip-flop being indeterminate.

(b). Propagation Delay. The clock input to either flip-flop should be a narrow, positive pulse with a minimum width of 20 ns at the 1.5 V amplitude point. The total delay from the time the data is present at the input to the flip-flop until the output of the flip-flop has changed states, is a sum of the clock pulse width and the propagation time to a logical "0" or "1." This time is a minimum of 20 ns for the clock pulse, plus an average of 30 ns for propagation time to a logical "0" or logical "1," giving a total sum of 50 ns. It can be seen that if the clock pulse is widened, the total delay is widened by the same amount. Since it is not desirable to operate the flip-flop at the maximum clock-frequency, it is advisable to use a minimum clock pulse-width of 25 ns. This will allow the clock pulse-width to jitter approximately 20 percent without reaching the minimum clock pulse-width. By feeding the clock pulse into the same gate as the J and K inputs, the J and K input data does not have to be present until the leading edge of the clock pulse. To allow the data to propagate through the flip-flop, the inputs must be present at least as long as the clock pulse is present. The "preset" and "clear" inputs present a load equal to two gates. Using a clock pulse that is 20 ns wide, and allowing the maximum 50-ns propagation time to a logical "1" or "0," the maximum toggle frequency is 14.28 MHz, with no time for propagation through wiring external to the network. Using a clock pulse of 20-ns width, a pulse spacing of 100 ns, and the maximum 50-ns propagation time to a logical "1" or "0," 30 ns remain for propagation through the wiring external to a network. This would allow 30 feet of external wiring with a propagation-delay rate of 1 ns per foot.

(4). Type SN5470

(a). Circuit Description. The second basic type of flip-flop is the SN5470, which is a single-phase, JK flip-flop. A logic diagram of the SN5470 is shown in Figure 1-50. The same symbols are used here as in the SN5472 and -73 flip-flops. The inverters on the J* and K* inputs, and gates A and A' make up the gates to the flip-flop.† Gates E and E' provide the outputs. Gate F is a buffer circuit for the clock input and limits the load on the clock input to the equivalent of one gate-load. The gates B, B', C, and C' make up the master portion of the flip-flop. Gates D and D' make up the slave portion of the flip-flop. Transistors T_1 and T_2 control the

† TI Series 54/74 Integrated Circuits, William A. Stover, ed. (Dallas: Texas Instruments Incorporated) p. 45.

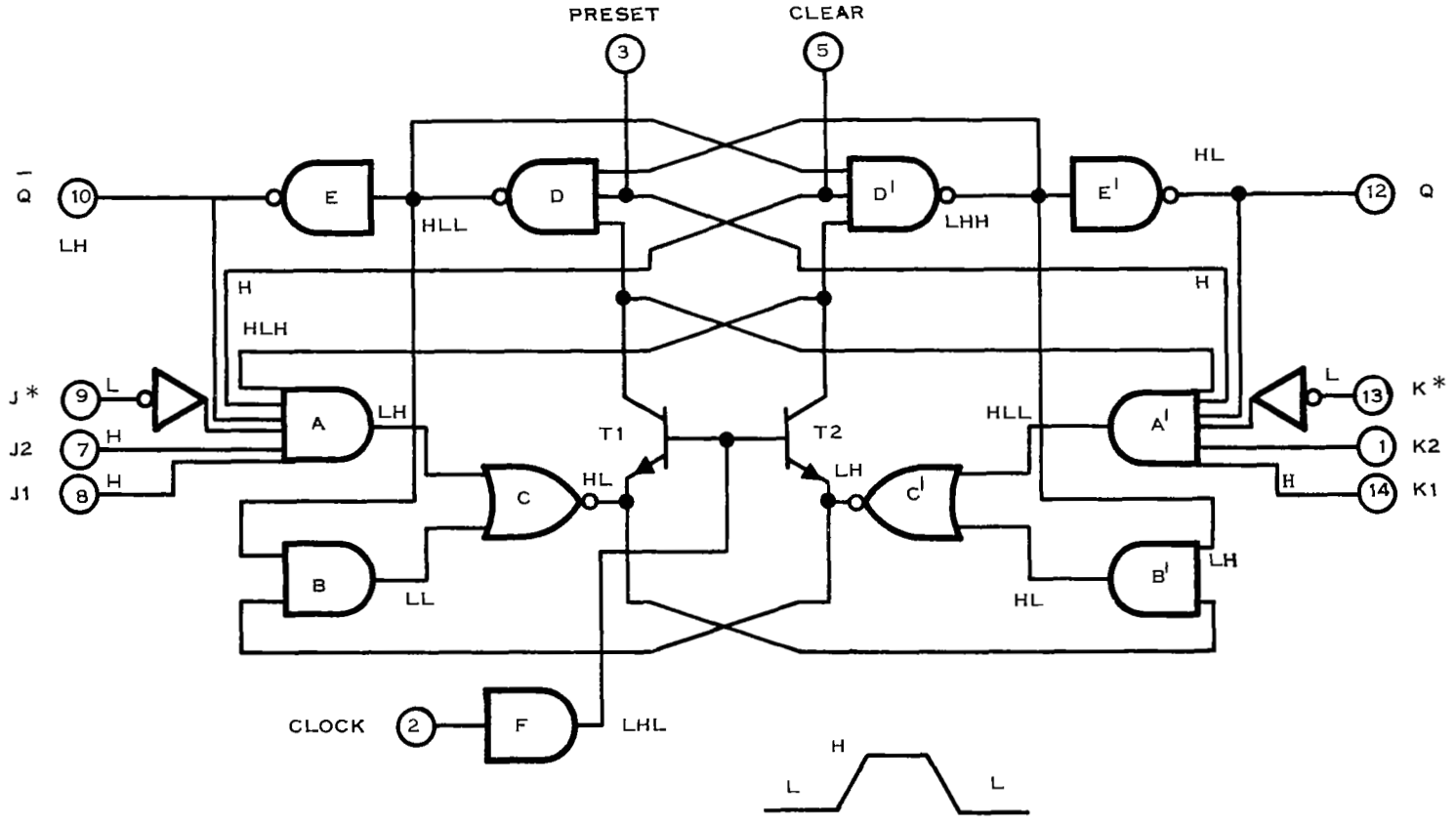


Figure 1-50. Logic Diagram for a TTL Single-Phase J-K Flip-Flop (SN5470)

transfer of information from the master portion to the slave portion of the flip-flop. The "preset" and "clear" inputs are normally,"high" but a "low" on either of these lines causes the flip-flop to be preset or cleared.

(b). Circuit Analysis. As an example of the operation of the flip-flop, assume that the Q output is "high," the J_1, J_2, K_1, and K_2 inputs are "high," the J* and K* inputs are "low," and both "preset" and "clear" inputs are "high." Before the start of the clock pulse, gates A, B, C', D', and B' are "low." The remaining gates C, D, and A' are "high." Gates E and E', the outputs of the flip-flop, are "low" and "high," respectively. During the clock pulse, transistor T_2 is turned "on," which causes one input of D' to go "low," forcing the output "high." The feed-back from the output of D' into gate D makes the output of D change to a "low" level. The output of D' is also fed into B'. This D' output, along with the "high" output from gate C, causes the output of B' to go "high." As B' is going "high," E' is going "low," which in turn causes A' to go "low"; but, the output of C' remains "low," since one of its inputs is still "high." At the end of the clock pulse, the output of gate E is "high," meaning that all inputs to A are "high," which forces the output of A to be "high." The output from A is fed through gate C to cause a "low" at the output of gate C, forcing the B' output "low" and causing C' to go "high." The states of gates C and C' remain fixed until the next clock occurs, because of the latching action of gates B and B'. After the clock pulse, A' remains "low" because the output of E' is "low." Since gates D and D' are "low" and "high," respectively, the outputs E and E' are "high" and "low," respectively. This series of actions causes the Q output to go "low" and $\overline{Q}$ output to go "high" while the J and K inputs are "high."

The "preset" or "clear" inputs should only be used when the clock line is "low." If the clock input is "high" when the "preset" or "clear" line is "low," the Q and $\overline{Q}$ outputs could go "low" at the same time.* If, for instance, it is desired to set the Q output "low" by means of a "low" at the "clear" input, the output of gate D' would be forced "high." If the clock pulse now occurs, and if gate C output is "low," the output of gate D will be forced "high," and since both D and D' are "high," E and E' will be "low." If the clock pulse does not occur, then gate D' will cause D output to go "low," and the $\overline{Q}$ output would then be "high" and the Q output would be "low." When either the "clear" or "preset" input goes "low," either gate A or gate A' is disabled by the feedback from the "clear" or "preset" inputs. This prevents data at the J or K inputs from interfering with the changing of the flip-flop during the "preset" or "clear" cycle. Gates D and D' are also fed back to gates B and B' respectively, to insure that the latch consisting of gates C and C' does not change states. One of the gates, C or C', will always be "high" and the other will always be "low." Conditions could occur on the J or K inputs which would cause this latch to try to change states. However, the gate, which is initially in the "0" state, cannot be fed back to latch the other gate because either D or D' will block gate B or B'. The

---

* Ibid. p. 114.

feedback from the Q and $\overline{Q}$ outputs of the flip-flop into the K and J inputs, prevents the J input from being enabled when the Q output is "high," and prevents the K output from being enabled when the $\overline{Q}$ output is "high."

(c). Propagation Delay. The clock pulse must be a minimum of 20 ns wide, which is the same as for the SN5472 and -73 flip-flops. Again, as a practical matter, it would be advisable to keep the minimum clock pulse width at 25 ns to allow for some jitter in the clock pulse width. The maximum propagation time to a logical "0" or "1" is 50 ns. Therefore, the total delay through the flip-flop is 15 ns for setup time, plus 50 ns propagation time, or a total of 65 ns. This is equivalent to a toggle frequency of approximately 15.4 MHz. Operating the clock with a period of 100 ns leaves a minimum of 35 nanoseconds of propagation time external to the flip-flop.

E. SYSTEM APPLICATIONS

1. General

By using microcircuits in a digital design, a large portion of system design is eliminated. With conventional components, the logic design is done with logic equations and symbols without regard to the actual circuit. The circuit designer then designs circuits that will implement the required logic functions. However, the circuit-design effort is essentially eliminated when the logic design is based on using available monolithic logic microcircuits. Stated simply, the system designer connects sub-assemblies in a specified functional design. In order to interface several hundred, and in some cases thousands of circuits, the designer must have information and data on the devices. This information is supplied on the device manufacturer's data sheets. Knowing how to use microcircuit data sheets, and understanding the information given and the limitations of the data sheets, is the beginning of correctly using logic micro-circuits within a system.

2. Using Manufacturer Data Sheets

Manufacturer data sheets are the specifications that are used to describe and characterize a product. A microcircuit's data sheet contains such information as a brief description of the circuit, schematic and logic diagrams, absolute maximum ratings, performance and electrical characteristics, test conditions, typical values and curves, and package dimensions.

There is a wide variation between the data sheets of one microcircuit manufacturer and those of a different manufacturer. And unfortunately, a portion of the information shown on a data sheet may be more in the nature of advertisement material than useful design information. Therefore, in many cases, the system designer must obtain more information from the device manufacturer or perform

additional device testing. Very few application guides and rules are placed on the data sheets. In some cases, only typical values of certain electrical parameters are given. It is well known that a designer cannot design using typical data. Typical values are useful to the designer when given with the minimum or maximum limits. But, often the typical values were established using prototype circuits and thus do not represent the typical values of the present production units.

The EIA Registration Data for Semiconductor Integrated Logic Gating Circuits gives some indication of the type of information that should be on data sheets. Several typical data sheets were presented and described in the preceding discussion of examples of digital circuits. Other data sheets from different manufacturers are presented in the Appendix.

The following general statements should be considered when using micro-circuit data sheets:

- The user should be sure that the data sheets he has represent the latest information about the device. Data sheets are released at the time production of the circuit begins, and sometimes before. By the time mass production has begun and the circuits have been used in actual system application, several changes may have been made in the circuits—changes that won't be reflected on earlier data sheets.
- The schematic diagram on a data sheet does not usually show the isolation diodes associated with the components. Some thought should be given to the significance of these diodes, especially when interfacing between discrete-component circuitry or combinning different logic families. Also, the component values shown on the schematic diagram are typical values and will vary as much as ±20 percent between different circuits.
- The absolute maximum ratings should never be exceeded when testing the device or in system application. The absolute maximum voltages given on data sheets represent breakdown voltages of certain components, such as isolation diodes and base-to-emitter or -collector junctions.
- The recommended operating conditions given on the data sheet should always be used in system application. The recommended supply voltage range was used to characterize the device and also was used for the manufacturer's final electrical test. This does not mean that the circuits will not operate at other voltages, but they will not necessarily meet the parameter limits specified on the data sheets.

- The test conditions used for testing the electrical parameters are representative of worst-case conditions. Those test conditions may not be exactly equal to the worst-case conditions of a given system. The actual worst-case conditions of the system should be considered when examining data sheets.

3. Application Guides and Rules

a. General

Users of microcircuits have a difficult and complex task to perform when they must choose and evaluate the various types of available logic circuits. After the particular family has been chosen, the user must be capable of correctly applying the circuits in a system. General guidelines and rules for system applications are difficult to define because each system will have different requirements of speed, power, noise immunity, reliability cost, size, weight, etc. A basic rule that applies to all monolithic microcircuits is as follows:

RULE

Use the individual circuit in the application for which it was designed.

In other words, use the circuit with straightforwardness of application, avoiding tricky, unnatural hookups that are intended to save one or two microcircuit devices. Experience has borne out that the time and dollars saved by using nonstandard design techniques have been lost many times over during system-checkout effort. With design experience in using a particular microcircuit family, and by using good digital design practices and application rules, it is possible to eliminate the majority, if not all, of the breadboarding previously required for a digital system.

The use of application rules to improve the overall reliability of a system is very familiar to system designers. Derating rules have been used for years in improving the reliability of circuitry using discrete components. However, derating rules, as they apply to transistors, diodes, and other discrete components, cannot be applied in the same way to microcircuits. The power dissipated by a resistor or the forward current of a diode can be derated to a low value to provide a more reliable application. Whereas, a microcircuit's operating parameters cannot be derated in system application. Actually, the stress of the individual monolithic components within a circuit are derated during the initial design of the microcircuit.

There are certain application guides and rules that can be applied to microcircuits to provide a more reliable system. These application guides and rules can be divided into two groups: rules that apply to all digital microcircuits, and more specific rules that apply to a particular family or device.

General application rules have been discussed in the previous portions of this section. They pertained to rules for selecting a microcircuit family, definitions of digital microcircuit parameters, and guides for using microcircuit data sheets. They will be summarized here along with other general applications guides and rules:

- Become familiar with the available microcircuits. Know the limitations of the devices and the fabrication techniques. There are many factors that affect the yield, cost, and reliability of a device, that should be known before trying to apply microcircuits in a system application.
- The fan-out capabilities of a circuit should be defined in terms of current rather than to merely use a number. Very few applications require the full fan-out ability of a circuit, especially in the DTL or TTL families. However, in system applications, the maximum allowable fan-out should be decreased by one or two equivalent loads to take into account the wiring capacitance, temperature variations, and other system effects.
- Switching speed is an important parameter of microcircuits and should be given special consideration in system design. The switching times are difficult to test when using automatic equipment, especially at temperature limits. The switching times shown on data sheets are given for 25°C only, and sometimes they are tested only on a sample basis. Therefore, a logic circuit should not be operated near its maximum switching speed. A curve showing the switching speed versus temperature should be obtained either by laboratory testing or from the device manufacturer. Rules for the maximum number of series-connected gates between clocked flip-flops as a function of operating frequency should also be established.
- The primary power supply for microcircuit logic applications is typically a low-voltage, high-current unit. Power requirements can be safely estimated using data-sheet power consumption figures. These figures are usually given for a full fan-out condition, which is conservative for most system applications. As expected, high-quality, precise regulation of the dc supply voltage is not a requirement in most digital systems. However, a low output impedance is required to keep variations in load and switching-current transients from creating

voltage-level changes, which may be seen as "noise" by some elements, especially flip-flop clock inputs. Also, a low power-supply ripple is desirable for the elimination of another source of "noise", (which can build up to values approaching the element thresholds),namely, logic noise created by the system itself. Supplies should be adequately decoupled by using large-valued tantalum capacitors for low-frequency noise, and ceramic disk capacitors or equivalent for high-frequency noise. Additionally, the V_{CC} lines in the logic section should be decoupled either on each individual card or by banks of cards, depending upon the particular application. Ground lines should be substantial, to the point of using solid copper busses in large systems, to keep noise on ground at a minimum and to keep the reference level (ground) to each element as nearly equal as possible throughout the system.

Microcircuit manufacturers publish some application bulletins or reports on their respective devices. They usually contain only a basic description of the circuits and several design applications for using the circuits in systems. They seldom contain specific application guides and rules.

Specific application guides and rules are usually established by system manufacturers who have actually used the devices in operating systems. Some of these rules have been passed back to the device manufacturer and used for corrective action to improve the device. However, certain application guides, or "do's and don'ts," are collected and maintained by the system manufacturer. Many of these application guides and rules are considered proprietary information within the company. There is as much competition between system manufacturers using microcircuits as there is between microcircuit manufacturers. Therefore, the microcircuit users consider that the advantages they have gained through their application experience in using microcircuits would be lost if certain application guides and rules were published.

b. Recommended Loading Rules and General Application Guides for the Series 51B, RCTL Families of Microcircuits

The earlier digital families (RTL or RCTL) require much more application information than the later families (DTL and TTL). Although Series 51B data sheets are not presented in this handbook, they should be referred to when using the collection of specific application rules for certain families of digital microcircuits which will be presented hereafter. The following definitions pertain to the recommended loading combinations shown in Tables 1-6 and 1-7:

- Unit dc load—any input to a Series 51B Gate; input to the SN517B; input to the SN518B; any "preset" or "clear" input to a Series 51B flip-flop; control line inputs to the SN5191B.
- Unit ac load—clock input to a Series 51B flip-flop; counting inputs to the SN5191B.
- Logic inputs (R and S inputs) to Series 51B flip-flops must be considered as a special case; a hybrid type of load.

Table 1-6. *Recommended Loading Combinations for Series 51B Gates, SN518B, and SN5191B

Combination	Collector Output			Emitter Follower Output		
	Minimum dc	Maximum dc	Maximum ac	Minimum dc	Maximum dc	Maximum ac
1	1	4	1	-	0	0
2	1	3	2	-	0	0
3	1	1	3	-	0	0
4	-	5	0	-	0	0
5	-	0	0	-	25	0
6	-	0	0	5	23	1
7	-	0	0	5	21	2
8	-	0	0	5	19	3
:	:	:	:	:	:	:
:	:	:	:	:	:	:
14	-	0	0	5	7	9
15	-	0	0	5	5	10

* Note: Refer to Notes 1 through 4 in series of notes following this table.

The following special notes pertain to Tables 1-6 and 1-7:

1) A 20 kΩ resistor from the collector output to ground may be used to satisfy the minimum dc loading requirement.

2) If the ac loads are flip-flop clock inputs, the driving output must be in the "low" voltage state during any and all negative transitions at the flip-flop logic inputs (R and S inputs).

Table 1-7. †Recommended Loading Combinations for Series 51B Flip-Flops (Sheet 1 of 2)

Combination	Q		$\bar{Q}$		Q*		$\bar{Q}$*	
	Maximum dc	Maximum ac	Maximum dc	Maximum ac	Maximum dc	Maximum ac	Maximum dc	Maximum ac
1	3	1	1	0	0	0	0	0
2	3	1	0	0	0	0	9	0
3	3	1	0	0	0	0	6	1
4	3	1	0	0	0	0	3	2
5	3	1	0	0	0	0	0	3
6	2	2	1	0	0	0	0	0
7	2	2	0	0	0	0	9	0
8	2	2	0	0	0	0	6	1
9	2	2	0	0	0	0	3	2
10	2	2	0	0	0	0	0	3
11	0	3	1	0	0	0	0	0
12	0	3	0	0	0	0	9	0
13	0	3	0	0	0	0	6	1
14	0	3	0	0	0	0	3	2
15	0	3	0	0	0	0	0	3
16	4	0	4	0	0	0	0	0
17	4	0	0	0	0	0	20	0
18	0	0	0	0	20	0	20	0
19	0	0	1	0	18	1	0	0
20	0	0	1	0	16	2	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
27	0	0	1	0	2	9	0	0
28	0	0	1	0	0	10	0	0
29	0	0	0	0	18	1	9	0
30	0	0	0	0	16	2	9	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
37	0	0	0	0	2	9	9	0

Table 1-7. †Recommended Loading Combinations for Series 51B Flip-Flops (Sheet 2 of 2)

Combination	Q		$\bar{Q}$		Q*		$\bar{Q}$*	
	Maximum dc	Maximum ac	Maximum dc	Maximum ac	Maximum dc	Maximum ac	Maximum dc	Maximum ac
38	0	0	0	0	0	10	9	0
39	0	0	0	0	18	1	6	1
40	0	0	0	0	16	2	6	1
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
47	0	0	0	0	2	9	6	1
48	0	0	0	0	0	10	6	1
49	0	0	0	0	18	1	3	2
50	0	0	0	0	16	2	3	2
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
57	0	0	0	0	2	9	3	2
58	0	0	0	0	0	10	3	2
59	0	0	0	0	18	1	0	3
60	0	0	0	0	16	2	0	3
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
67	0	0	0	0	2	9	0	3
68	0	0	0	0	0	10	0	3

† Note: Refer to Notes 2, 3, 6 and 7 in series of notes following Table 6.

3) If the ac loads are flip-flop clock inputs, and if any of the flip-flops being driven is permitted to accept the R = S = 0 logic condition (negative logic) or one of the conditions given in the first tabulation shown hereafter, no dc loads may be simultaneously driven from the output, and the output voltage should be clamped by connecting the appropriate resistor between the collector output and ground. (See the second tabulation shown hereafter.)

Condition	Rn	Sn	Qn	$\overline{Q}$n
A.	1	0	0	1
B.	0	1	1	0

Microcircuit Device Category	AC Loads from Collector Outputs		AC Loads from Emitter-Follower	
	V_{CC} = 3 V (kΩ)	V_{CC} = 6 V (kΩ)	V_{CC} = 3 V (kΩ)	V_{CC} = 6 V (kΩ)
Gates, SN517, SN518, SN5191	5.9	2.7	10.0	5.0
Flip-flops	8.0	3.2	–	6.0

4) If the ac loads are flip-flop clock inputs, refer to Figure 1-51 and to the following rules.

- For collector outputs, N = 1 dc load.
- For emitter-follower outputs, N = 9 dc loads or 3 ac loads or a combination of ac and dc loads, using the rule that N_{MAX} = 9 dc loads, and 1 ac load = 3 dc loads.

5) If ac and dc loads are driven from the same output, flip-flop logic inputs (R and S inputs) should be considered as zero dc loads for minimum load restrictions, and as one dc load for maximum load restrictions. If only dc loads are driven from the output, R and S inputs should be considered as 1/5 dc load (except for counting for the Note No. 4 restriction, where R and S inputs should be counted as one dc load.)

6) If ac and dc loads are driven from the Q output, flip-flop logic inputs (R and S inputs) should be considered as one dc load. If only dc loads are driven from the Q output, R and S inputs should be considered as 1/5 dc load. For all combinations of loading at $\overline{Q}$ and $\overline{Q}$*, R and S inputs should be counted as one dc load, except for combination 16, 17, 18, where they represent 1/5 dc load.

7) Only one-half of the total number of loading combinations have been presented. The rest of the combinations may be obtained by relabeling the columns: Change Q to $\overline{Q}$, $\overline{Q}$ to Q, Q* to $\overline{Q}$*, and $\overline{Q}$* to Q*.

The following definitions are miscellaneous application guidelines:

- Unused gate inputs: 1) Ground unused gate inputs, or 2) Connect unused gate inputs to active inputs of the same gate to satisfy minimum loading requirements.
- Unused "preset"/"clear" inputs of flip-flops should be grounded.
- Unused logic inputs of flip-flops should be connected to V_{CC}.
- The logic inputs of flip-flops should not be tied to a potential that is less than +30 mV with respect to ground. Outputs of all devices of the Series 51B family will always be ≥ 30 mV above ground.
- "Clock"/"preset" and "clear" relationships:
  - For reliable "preset" operation, a minimum time (T_1 as defined in Figure 1-52 must be allowed between the negative transition of the "clock" input and the negative transition of the "preset" pulse. The value of T_1 is a function of the method of operation of the flip-flop. For cases 1, 2, and 3 which follow, refer to Figure 1-52:
  - Case 1 If the flip-flop is connected in the toggle mode (R connected to Q, S connected to $\overline{Q}$), $T_1 \geq 4\ \mu s$.
  - Case 2 If R is at a logical "1" ("low" voltage input) throughout the time T_1, then $T_1 \geq 10\ \mu s$.
  - Case 3 If R is at a logical "0" ("high" voltage input) for at least 1 μs during T_1, $T_1 \geq 4\ \mu s$.

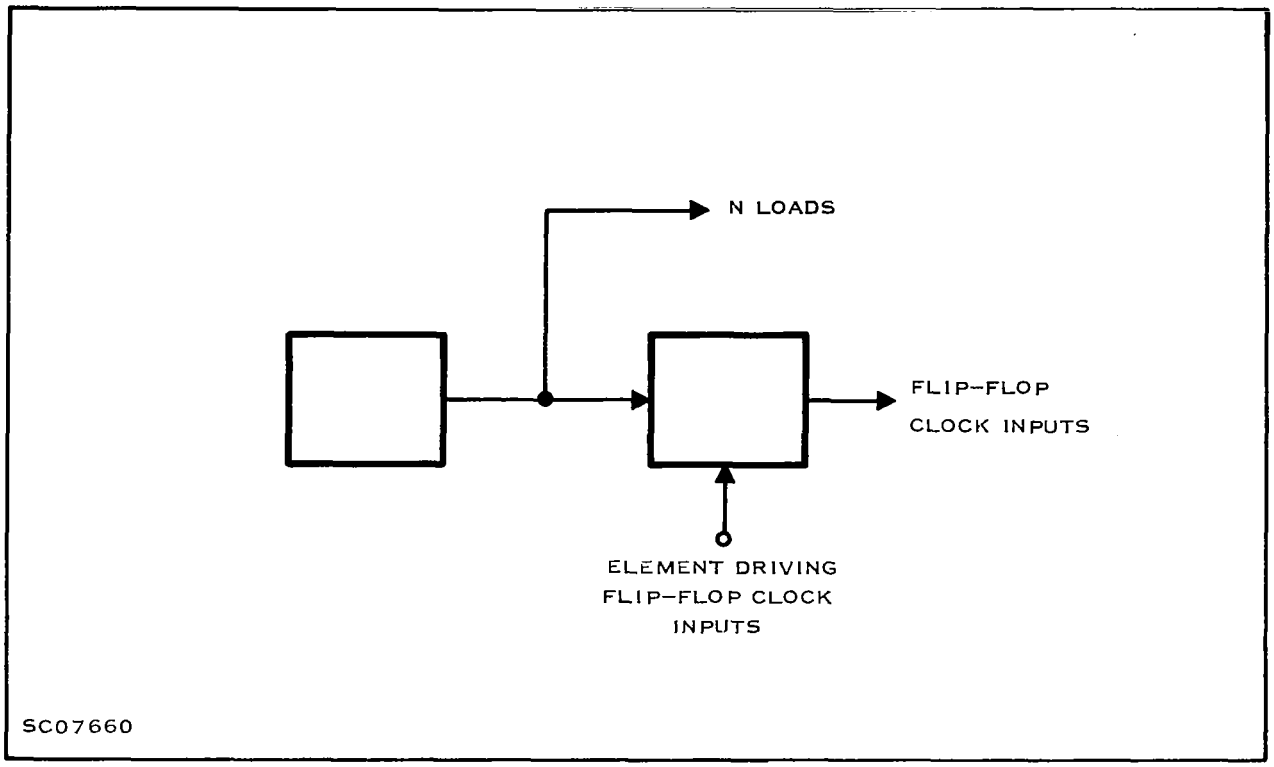


Figure 1-51. Block Diagram for Flip-Flop AC Loading

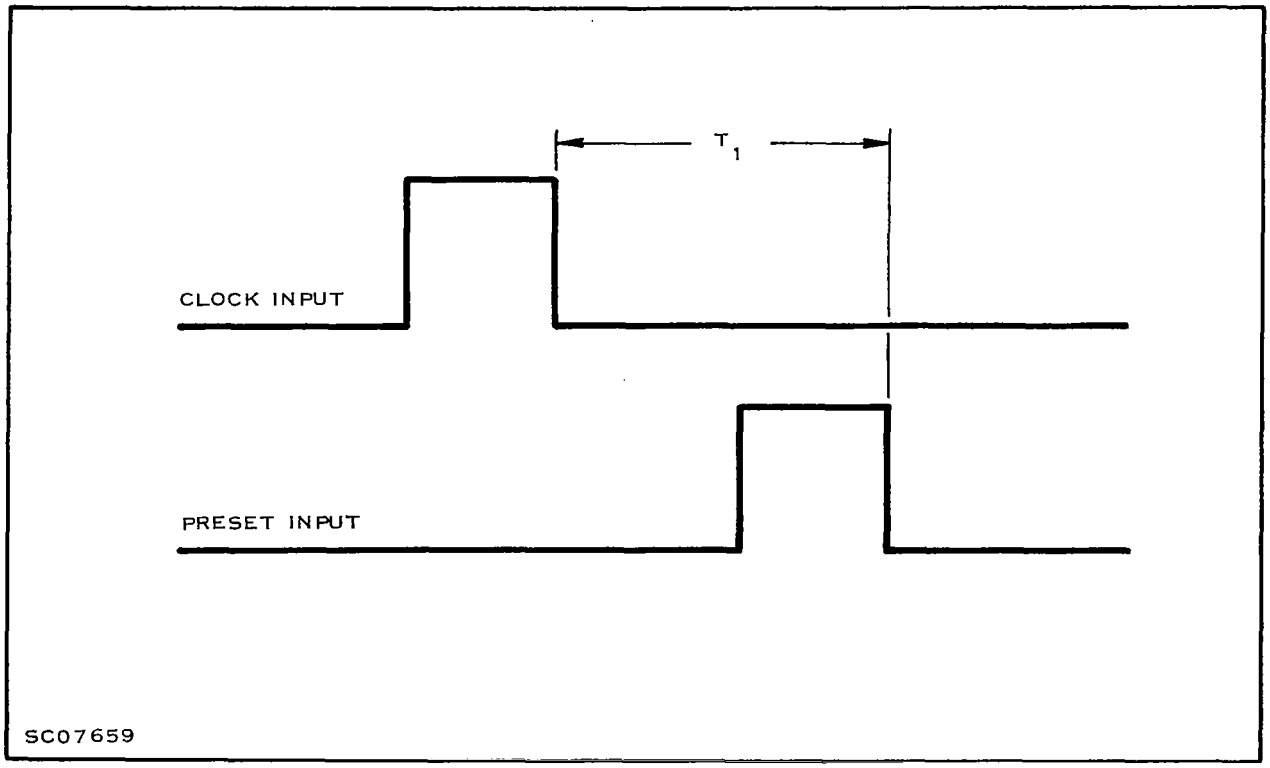


Figure 1-52. Minimum Time T_1 Defined for Reliable "Preset" Operation

For any cases not covered here, use $T_1 \geq 10\ \mu s$. If $T_1 = 10\ \mu s$ is an unacceptable condition for cases not covered here, device design engineers should be supplied with sufficient information to run an evaluation to define T_1.

- If the "preset"/"clock" phase relationships are as defined in Figure 1-53, no special problems will be encountered. (T_1 restriction does not apply.) The only rules that should be followed in these cases is that "preset" pulse width ≥ 500 ns and minimum time between removal of "preset" and negative edge of "clock" pulse = 1 μs.

c. Guide Rules for System Design and Layout When Using DTL and TTL Digital Microcircuits

Several rules that have been established through system experience with DTL and TTL digital microcircuits will now be presented. They pertain more to system design and layout than to "do's and don'ts" which apply to a specific device. The guide rules are as follows:

- Because of the high speeds of these device families, ac noise signals will propagate through the gates unless the system has a proper ground. Very large surface areas should be used in the ground system, not particularly to carry the dc current, but to carry the high-frequency component of the current. Every effort must be made when designing the printed circuit board (PCB) layout to insure the widest possible ground etch on the board. If at all possible, in PCB layout the ground should be distributed from both ends of the connector, and the leads to the ground bus should be as short as possible.

- It is considered good design practice to buffer all signal cables within a system by using a microcircuit inverter on each end. The output of signal-driving cables should not be reused as logic functions within the system unless buffered and compensated for propagation delay. Due to the input-output impedance mismatch of high-speed microcircuits, the output end of the cable should be terminated with a small resistor.

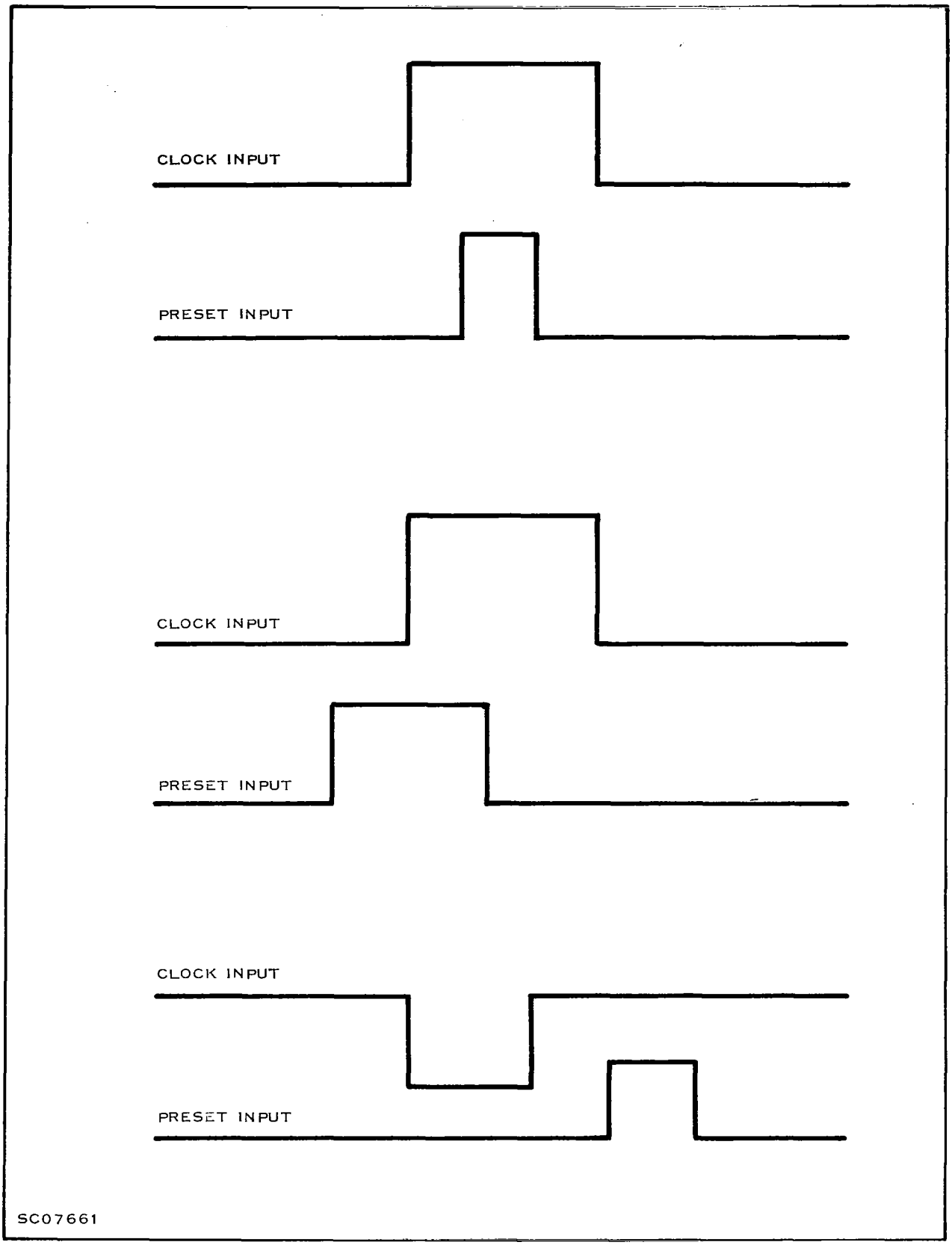


Figure 1-53. Preferred "Preset"/Clock Phase Relationships

- Unused inputs of the DTL and TTL circuits should not be left open. An open input will not only slow the propagation delay but will provide an easy input for noise. It has been recommended in the past to tie all unused inputs to the power supply voltage (V_{CC}). This is sufficient for DTL circuits; however, for TTL circuits, the breakdown voltage of the input transistor could possibly be exceeded.

- The absolute maximum rating for the input voltage is 5.5 V. With the supply voltages equalized in the range from 4.5 to 5.5 V, it is possible that voltage transients may exceed the maximum allowable input voltage. Thus, if V_{CC} is applied to unused inputs, the breakdown voltage may be exceeded. The breakdown voltage of the multi-emitter transistors is approximately 6 V. There are several methods for preventing damage to the inputs:

  - The use of redundancy to cover unused inputs. An example of this is shown in Figure 1-54. There is little if any fan-out penalty,because the fan-out is to the same gate. Also, little if any speed penalty exists.

  - Return all unused inputs to V_{CC} via a load resistor.

  - Cover unused inputs by grounding an inverter input to create a "1" generator,which is fanned-out to unused inputs. This is an appropriate way of dealing with unused "clear" and "preset" inputs to flip-flops, since redundant logic is not available.

  In general, the first method is preferable, since it does not require additional hardware, and it can be implemented with only very short wire lengths. Under no circumstances should unused inputs be left floating, because the floating inputs reduce switching speeds.

Microcircuits will provide a very reliable system when they are used in their intended application under the recommended operating conditions. There are very few application rules that need to be especially considered when using the DTL and TTL families. This is one of the inherent reliability advantages of microcircuits, and it is an important reason for selecting a DTL or TTL family for use in new system designs.

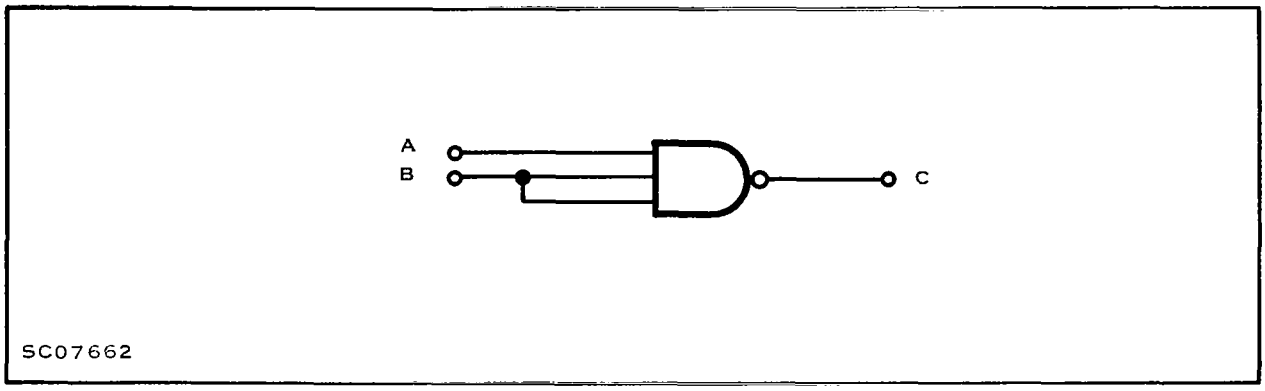


Figure 1-54. Redundancy Hookup for Unused Inputs

SECTION IV

LINEAR MONOLITHIC MICROCIRCUITS

A. LINEAR MONOLITHIC MICROCIRCUITS VERSUS LINEAR DISCRETE CIRCUITS

1. General

Linear monolithic microcircuits and their discrete-component counterpart may be compared in several ways, such as cost, reliability, size, and performance. The intent here is to more fully acquaint the reader with an overall comparison so that he may be better able to make the microcircuit-versus-discrete decision for a particular circuit function. Should the decision be to use the microcircuit format, then the following discussion should aid the reader in selecting the proper specification and in knowing what results to expect from the device.

The entire discussion will pertain only to monolithic-microcuit technology and will not delve into thin-film or metal-oxide-semiconductor (MOS) technologies. Henceforth, the term "monolithic microcircuit" will be taken to imply diffused resistors, diffused capacitors, and diffused transistors contained in the same silicon substrate and may be simply referred to as "microcircuit."

A very frequent question that is asked is, "Why are available, off-the-shelf linear microcircuits not nearly so numerous as digital microcircuits, and why have they only become available to a reasonable extent in the last three or four years, while digital microcircuits have been available in great varieties for a great deal longer?" While this question of linear versus digital may seem far removed from the stated purpose for this discussion, the answer will automatically lead into a detailed discussion of linear microcircuits.

The first and most obvious answer is that digital circuits lend themselves more to standardization, since most digital systems require a large number of identical gates, flip-flops, drivers, etc. On the other hand, systems utilizing linear solutions require a comparatively small number of circuits whose individual specifications are generally unique to the particular system. Therefore, it would be very difficult to create an "off-the-shelf" line of linear circuits that would satisfy all possible combinations of linear specifications such as gain, input impedance, function, frequency response, etc.

The second reason is that digital circuits are almost entirely composed of transistors and resistors. These two components are easily obtainable in monolithic form. However, linear circuits very frequently require transformers, capacitors, inductors, etc. which are difficult, if not impossible, to obtain in monolithic form. In other words, digital circuits have always been designed in a form that was readily adaptable to a monolithic format.

Finally, the tolerances and temperature coefficients of monolithic components are such that for many years it was believed that linear circuits; i.e., circuits whose output information is contained in the amplitude or shape of the output waveform, were not practical in monolithic form. On the other hand, digital circuits supplying simply a "yes" or "no" answer could easily be created, using worst-case design.

2. Linear Monolithic Microcircuit Constraints

The design of a particular linear microcircuit suffers from several constraints that do not generally hinder a design based on discrete components. These constraints are: circuit power dissipation, component values, component tolerances, types of components available for use, and the allowed degree of overall circuit complexity.

The circuit power dissipation is sometimes a problem in linear microcircuit design, since all the components are obviously contained in a very small area, and the problem of dissipating this heat away from the device or package is difficult. When a linear circuit is fabricated from discrete components, it is very easy to heat-sink one or several of the components dissipating the most power. In fact, discrete components capable of dissipating almost any specified power, or operating under any specified voltage, are readily available. Each of the many transistors contained in a single monolithic chip is capable of dissipating power at a rate comparable to that of commercially available small-signal discrete transistors such as the 2N2412 and 2N918. Likewise, each diffused resistor in the monolithic structure is thoroughly capable of dissipating as much as 1/4 W to 1/2 W of power. However, the problem here is not the individual component's power handling capability, but the power dissipation of the entire circuit. In fact, when an individual monolithic component is forced to dissipate an excessive amount of power, generally some other failure mode will occur before the component itself fails, such as burning open the lead pattern near the component. Total allowable power dissipation for a comparable discrete-component design is not given for obvious reasons, since this would depend entirely upon the choice of components from the wide variety possible, and the type of cooling provided.

Several components that are frequently used in linear circuit design are not available in monolithic form; they are: inductors, transformers, varactors,

tunnel diodes, and field effect transistors (FET). Very small, low-Q inductances can be achieved by making a portion of the metal interconnect pattern wind around in a planar spiral fashion. However, the low-Q and low-value inductances obtainable by such a method prevent its usage in monolithic microcircuits. It is used, however, in very-high-frequency, thin-film hybrid circuits. Field effect transistors that are N-channel have been fabricated within a monolithic microcircuit containing bipolar diffused transistors. However, the diffusion schedules necessary to fabricate the FET along with the bipolar transistors are not compatible; therefore; a separate diffusion is required for the FET. This, of course, forces the cost up and the yield down. It is for this reason that the FET is seldom seen in bipolar monolithic circuits, whereas it is most easily obtained from MOS technology. Likewise, the other devices mentioned, with the exception of the transformer, can conceivably be done in bipolar monolithic microcircuits, but the cost of doing so is prohibitive; therefore, it is not being done except in research laboratories.

The overall circuit complexity of the linear monolithic microcircuit is primarily dictated by the total power dissipation and the monolithic chip size. As the individual circuit chip increases in area, generally the yield will go down, due to the random defects across the silicon wafer being more apt to occur within the boundaries of the individual chip. This reduced yield, of course, raises the circuit cost. On the other hand, if the circuit design is made very simple, to keep the chip size down, a a point is reached where it is no longer advantageous from the cost and size standpoints, to make it in monolithic form, since the package size remains the same. Therefore, it follows that somewhere in between these two extremes, there is a point of optimum circuit complexity that will allow for the best choice of complexity from a cost standpoint. How this optimum point has changed over the past few years, until it is now at 40 to 80 components per circuit,is shown in Figure 1-55. The increase of component density with time is shown in Figure 1-56.

Since resistors, capacitors, and transistors are the primary monolithic components, the next part of this discussion presents a comparison of these elements with their discrete counterparts.

3. Component Comparison

a. General

The following discussion of monolithic microcircuit capacitors, resistors, and transistors is oriented toward linear design and will necessarily require some reference to the basic fabrication of each device. While fabrication structures were covered in an earlier section of this volume on applications, it is nevertheless believed that partially repeating the material at this time will be of extreme help in realizing the basic differences in monolithic and discrete components that affect linear circuit design.

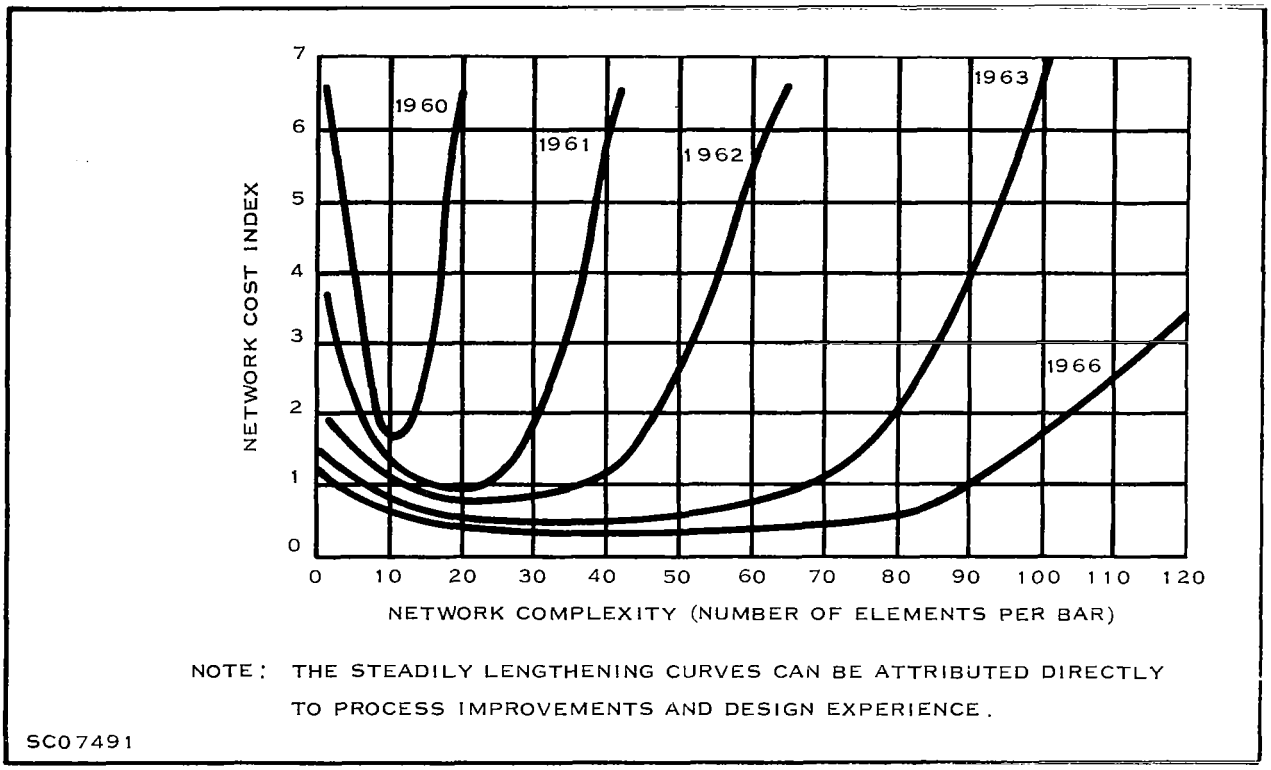


Figure 1-55. Effect of Network Complexity on Cost per Circuit Function

b. Diffused Resistors

The diffused resistors contained in monolithic microcircuits can be either P-type or N-type diffusion. However, the P type is prevalent in most microcircuits due to its higher resistivity. Resistors of the N type are sometimes used for very small resistances. A cross sectional view of typical P-type and N-type diffused resistors is shown in Figure 1-57. Diffused resistors of the P type and N type typically have a sheet resistance of 130 Ω/□ and 25 Ω/□ respectively. Since the P- and N-type resistors are actually base and emitter diffused, raising their sheet resistance requires a severe compromise of transistor parameters. The resistance is given in ohms-per-square because this, typically, is the most useful way of specifying a given resistance. This measurement unit means that, measured between two opposite edges, the square will have a given resistance independent of the dimensions of the square.

It is obvious at this point that the sheet resistance and the available area determine the upper limits on resistance value. If, for the moment, it is assumed that a given microcircuit chip is 50 mils square, and that half of this area may be used for resistors, there are about 1200 mils^2 for resistance after area for isolation has been subtracted. This means that for P-type resistors that are 1-mil wide, there is

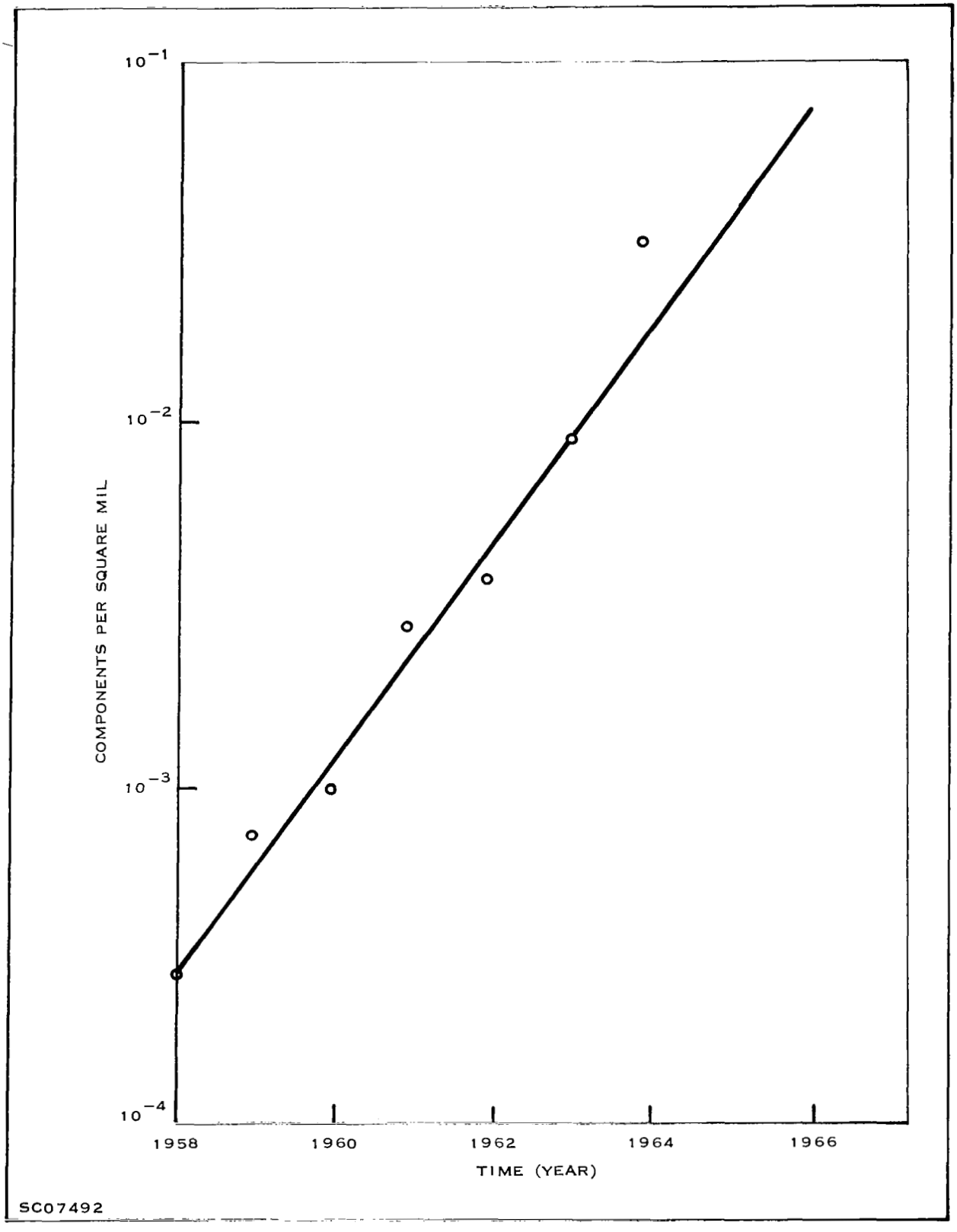


Figure 1-56. Increase of Component Density with Time

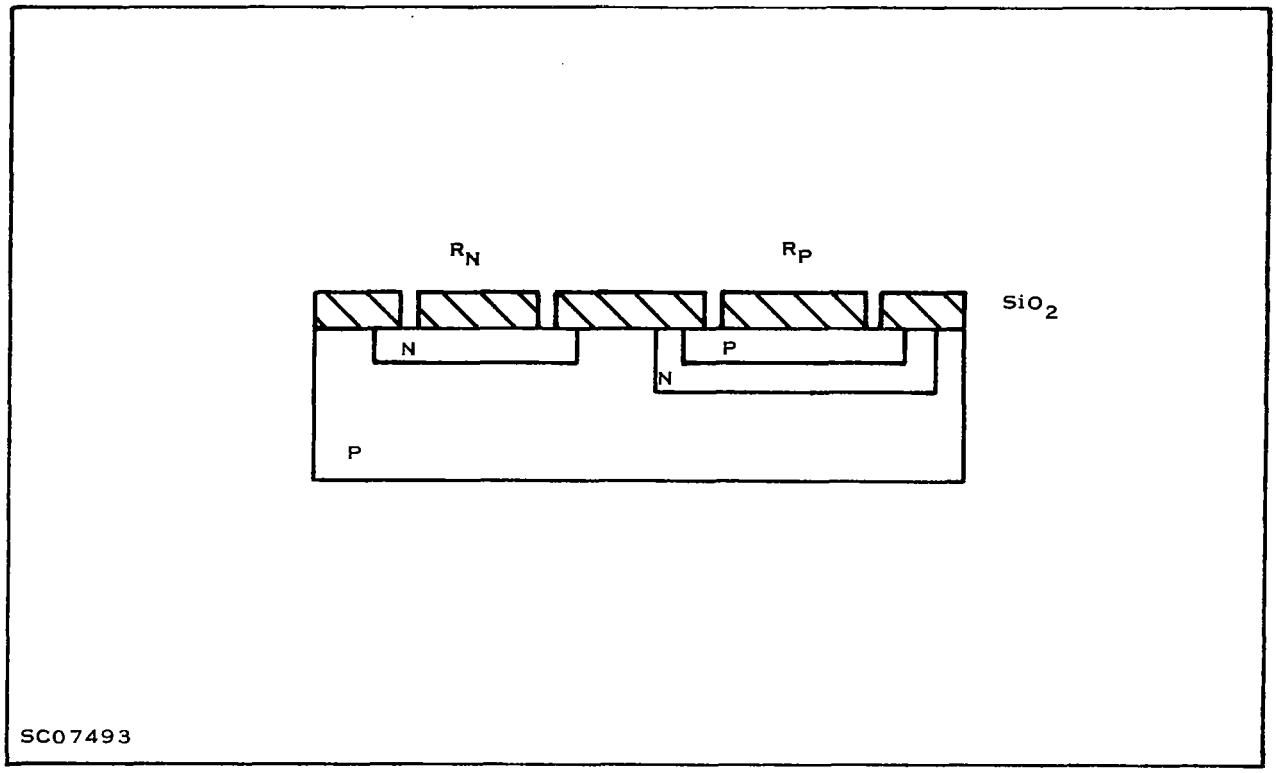


Figure 1-57. N-Type (Emitter Diffusion) and P-Type (Base Diffusion) Resistors

a total resistance of 150 kΩ, and for a resistor 0.5 mil wide, 300 kΩ. If much narrower resistors were used, this value could be raised. However, when this is done, a smaller error in the dimensioning of the resistor will result in a larger percentage error in the total resistance, which is, of course, a very serious problem in linear designs. Indeed, it is very difficult to make a direct comparison between the values of resistance available in monolithic and in discrete form, since discrete resistors may be obtained in any conceivable value, and diffused resistors can be made very large by making them narrow and fabricating a larger chip. For all practical purposes, it can be said that a monolithic diffused resistor will seldom exceed 20 kΩ.

The manufacturing tolerance on typical diffused resistors is approximately ±20 percent. This is caused by the difficulties of controlling the many factors affecting the sheet resistance. While this initial tolerance may seem to be unacceptable for linear design, the fact is, that since it is caused by variations in the sheet resistance, all the resistors on the same chip will rise or fall by approximately the same percentage. In fact, the resistance ratio of any two resistors on the same chip will either remain constant or vary by no more than ±1 to 2 percent over the initial tolerance range. By comparison, discrete resistors may be purchased to any desirable tolerance required for a particular design. However, one seldom designs a circuit requiring a tolerance of better than 0.1 percent.

Diffused resistors typically have a positive temperature coefficient of 1200 to 1600 ppm/C°. Fortunately, all the resistors on the same monolithic chip will have the same temperature coefficient, and the ratio of any two resistors will remain constant to 1 to 2 percent over production and temperature. A curve showing temperature variations of a typical P-type resistor of 130 Ω/□ sheet resistance is shown in Figure 1-58. The larger the sheet resistance, the larger the temperature coefficient. For a rough comparison, discrete resistors may be obtained that have either a positive or a negative temperature coefficient that is as low as 50 ppm/C°.

Consider, for example, the simple amplifier shown in Figure 1-59. Assume that initial tolerance or temperature has caused R_2 to be 10 percent above nominal. As pointed out previously, R_1 will also be approximately 10 percent high and thus will cause no change of the base bias-voltage. Since R_E will also be 10 percent high, the collector current will be reduced from nominal. However, R_L is also about 10 percent high. Consequently, the output dc level and gain (R_L/R_E) are as initially desired. Therefore, while the initial tolerance and temperature coefficient are definitely worse than in the discrete case, a circuit designed such that it depends on resistance ratios rather than resistance absolute value, as in Figure 1-59, would perform as nicely as if it had been done with tight-tolerance discrete components. In other words, careful design can eliminate the need for precision values and low-temperature coefficients for most purposes.

Each diffused resistor has several parasitic components associated with it. In general, they are of no consequence. However, to evaluate the performance of diffused resistors, it is necessary to discuss their parasitics and to be aware that they exist, since they are sometimes very important when used in a linear design. Illustrated in Figure 1-60 is an equivalent circuit for the P-type diffused resistor shown in Figure 1-57. Terminals 1 and 2 are the resistor terminals, and R_2 is the desired resistance. Resistor R_1 is the contact resistance associated with making the metal interconnection to the P-type material, and it would be about 2 Ω for a 1-mil resistor, and 5 ohms for a 0.5 mil resistor. The parasitic PNP transistor shown in Figure 1-57 consists of the P-type resistive material, the N-type isolation film and the P-type substrate material. To keep this parasitic transistor from affecting circuit performance, it is necessary to always tie the N film to the most positive supply voltage, and to tie the P substrate to the most negative supply voltage. Resistors R_3 and R_4 are the bulk resistances of the isolation region and substrate, respectively. These bulk resistances will be on the order of 100-to-300 Ω, and they are immaterial to the performance of the desired resistor, R_2, as long as the leakage currents are low, as in the normal case.

As is commonly known, wherever there is a PN junction that is reverse biased, there will be a depletion layer and a depletion-layer capacitance associated with this junction. Capacitances C_1 and C_2 are the depletion layer capacitances from the P-type resistor to the N film, and from the N film to the P substrate.

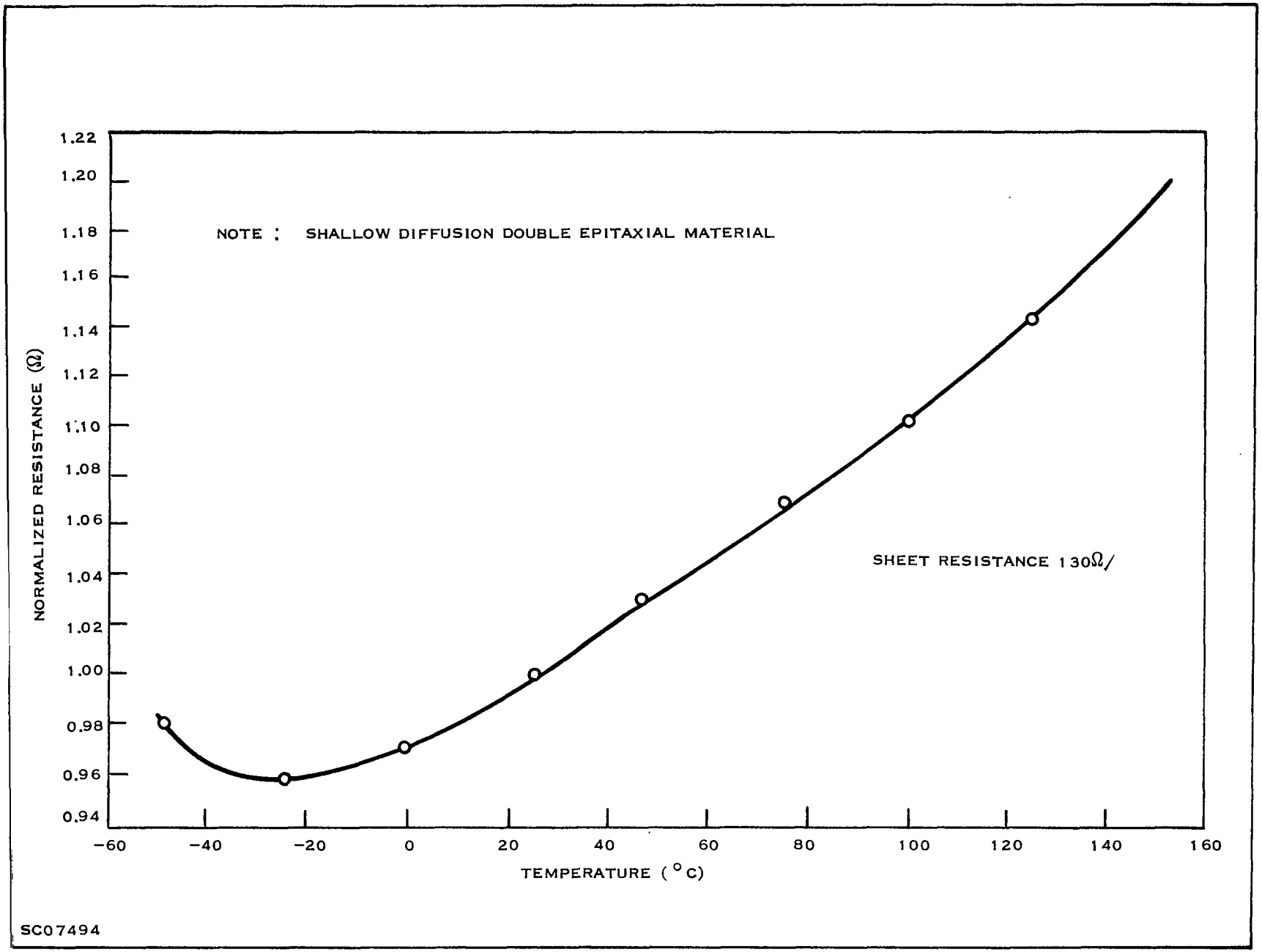
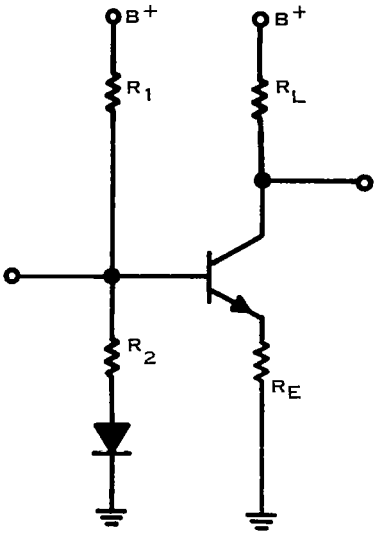
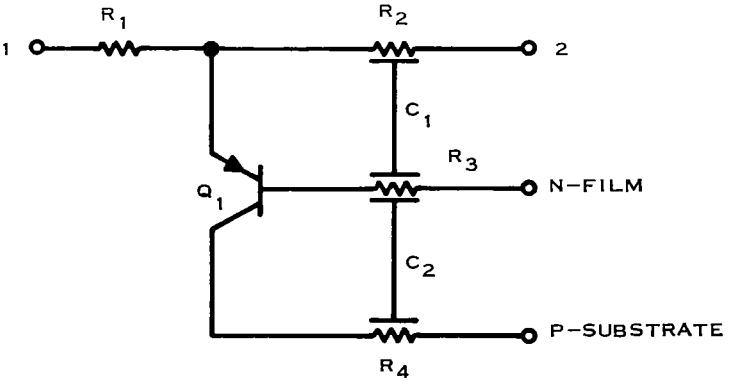


Figure 1-58. Typical Normalized Resistance versus Temperature



SC07495

Figure 1-59. Temperature-Compensated Amplifier



SC07496

Figure 1-60. Diffused Resistor Model

At high frequencies, it becomes important to consider this distributed-capacity effect of the resistor. Resistors with relatively small cross sections exhibit considerably less distributed capacitance than do wider resistors of equivalent value, since the distributed capacitance will vary in proportion to the square of the width of the resistor. To illustrate, assume that a 1.25 kΩ resistor is 1 mil wide. Neglecting contact areas, and using a 125 Ω/□ sheet resistance, the total resistor area will be 10 square mils, resulting in a total capacity of 3 pF. For a 0.5-mil wide resistor of the same resistance, the length would be 5 mils, and the area would be 2.5 square mils, resulting in a total capacitance of only about 0.7 pF. As can be seen, this value is only 1/4 the capacitance of the 1-mil resistor of equal resistance.

Discrete resistors do not have these parasitics. It should be pointed out, however, that even though some of these detracting factors seem overwhelming, diffused resistors are generally one of the closest approximations to a conventional resistor. The distributed capacity effect will not generally become a problem until frequencies in excess of 10 MHz are encountered.

c. Monolithic Bipolar Transistors

Monolithic bipolar transistors are very similar to small-signal discrete-component transistors, except for the larger bulk collector resistance and parasitic capacitances. Even these two disadvantages have been partially offset by the advent of the diffusion-under-the-film (DUF) and double-epitaxial processes. The larger collector resistance, and therefore, V_{SAT}, results from the necessity of having to make the collector contact at the surface of the device rather than at the backside, as in the discrete case. This forces the collector current to flow through a relatively long distance of high-resistivity collector diffusion. The N-collector diffusion cannot be made to have a low resistivity because this would lower the voltage level of the base-collector breakdown. Therefore, in triple- and quad-diffused structures, a compromise is made between breakdown and V_{SAT}.

The DUF structure approximates a back-contact collector, since the N^+ region is doped almost to the conductor level. Note, however, that the lightly doped material is still used for the collector to keep the breakdown voltage level up. Since monolithic transistors are isolated from one another by reverse-biased PN junctions, there will be inherent depletion-layer capacitances which will restrict the upper cutoff frequency. The amount of parasitic capacitance will obviously be a function of the area of the transistor. The DUF process and advanced photographic techniques have made it possible to fabricate transistors that are small enough to have cutoff frequencies that are just below the GHz level. To show the equivalent circuit at high frequencies for monolithic bipolar transistors, it is necessary to use a modified π-circuit model or a high-frequency T-circuit model in order to include the bulk-contact resistance and parasitic capacitance.

Monolithic transistors have beta and V_{be} variations with temperature that are almost identical to discrete-component transistors. However, the initial tolerance on beta or V_{be} is quite wide. Here again, this is generally of no consequence in a careful design because all transistors on the same chip will change approximately the same amount from nominal. In fact, these "automatically" matched transistors are one of the principal reasons for the successful performance of microcircuits in linear-circuit applications.

It would be very difficult to compare monolithic and discrete transistors, because there are so many types of discrete transistors. Some of the more important parameters of monolithic transistors are shown in Table 1-8. The comparison with discrete transistors will be left to the reader.

Table 1-8. Typical Monolithic Transistor Specifications

Parameter		NPN Transistor		Unit of Measure
		Type 1*	Type 2†	
BV_{CEO}		20.00	15.0	V
V_{SAT}	I_C = 1.0 mA	0.75	0.2	V
h_{fe}	I_C = 1.0 mA	80.00	100.0	–
h_{fe}	Match	15.00	15.0	%
V_{BE}	Match	3.00	2.0	mV
V_{BE}	Track	7.00	5.0	μV/C°
f_t	at I_C = 1.0 mA	60.00	–	MHz
BV_{CBO}		30.00	40.0	V

* Type 1: Triple- and quad-diffused, single epitaxial.

† Type 2: Double epitaxial and diffusion-under-film.

Both NPN and PNP transistors are available within the same monolithic structure, which is known as the quad-diffused structure. Presently, most microcircuit design activity is concerned with the NPN type. There are two primary reasons for this: the NPN technology is better known today, and when using the epitaxial or diffusion-under-the-film techniques, only one type, generally NPN, may be used.

d. Microcircuit Diffused Capacitors

As indicated in the previous paragraphs, both diffused resistors and transistors approximate quite closely their discrete counterparts. The integrated diffused capacitor differs considerably from the other components. The circuit model is quite complex, as shown in Figure 1-61, and does not approximate a discrete ideal capacitor. Once again, the capacitance obtained from a diffused capacitor is the depletion-layer capacitance between a P and N region under reverse bias. The diffused capacitors contain large parasitic components, both resistance and capacitance, and are

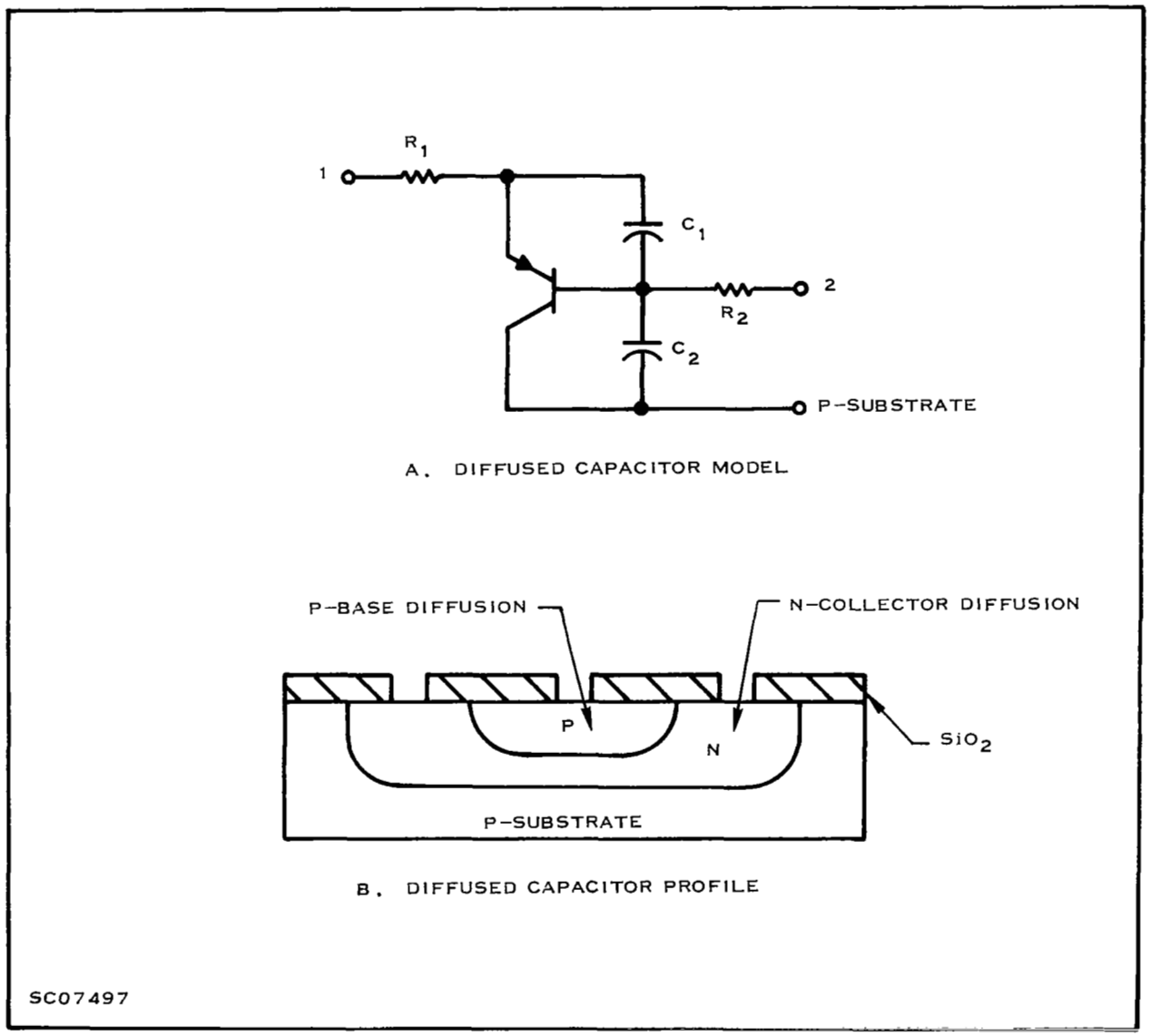


Figure 1-61. Integrated Diffused Capacitor

lossy, leaky, voltage-dependent, and unstable. The series resistor R_1, which is the bulk resistance of the P-type diffusion, accounts for the lossiness of the capacitor and the resultant low Q, since this resistance occurs between the contact and the effective capacitance area. This resistance would depend on the size of the capacitor and would typically be 20 Ω to 50 Ω. Resistor R_2 is the bulk resistance of the N material between the junction and N-contact area. This N material has a lower resistance than the P material and is, therefore, generally about 10 Ω. Capacitor C_2 is a parasitic capacitance that occurs due to the isolation-to-substrate junction, and it is approximately equal in magnitude to 1/2 the value of C_1, the desired capacitance between terminals 1 and 2. The capacitance generally obtained by such a diffused structure is about 0.2 pF/mil^2. If one were to assume that a monolithic circuit is 50 square mils in area, which is an optimum size in today's technology, it would be found that a 100 pF capacitor would require 1/5 of the total circuit area. In other words, a reasonable upper limit for diffused capacitors would be 100 pF to 200 pF.

If the diffused capacitor is to be used as a coupling capacitor, careful consideration should be given to the drive capabilities of the preceding circuit, which must drive the load impedance of the following stage and the capacitor parasitic capacitance, C_2. Capacitor C_1 must also always remain back-biased.

The fact that the usable capacitance is derived from a back-biased diode junction makes it obvious that the capacitor will be leaky, since leakage currents will flow identically as in reverse-biased diodes. This leakage current will be temperature dependent, as in normal discrete diodes.

The initial tolerance of diffused capacitors is ±20 percent, due to the fact that the depletion-layer capacitance is affected by the doping level in both the N- and P-type regions and is difficult to control. In addition, these diffused capacitors are voltage dependent because of the dependence of depletion-layer width on reverse-bias voltage. In other words, the bias voltage essentially varies the capacitor gap. The relationship between the diffused capacitance and reverse-bias voltage is shown in Figure 1-62. Generally, a diode in a microcircuit is simply obtained by using one of the five possible configurations offered by the transistor, as shown in Figure 1-63. This is done because transistors are to be formed elsewhere, and using them as diodes is more economical than diffusing specialized diode structures.

The connections shown in Figures 1-63(c), (d), and (e) have reverse breakdowns, dictated by the emitter-base junction, which will occur at 5.5 to 6.5 V. The value of voltage breakdown for the connections shown in Figures 1-63(a) and (b) is the collector-base breakdown voltage, and it would be 30 to 50 V, depending on the transistor structure. All the configurations have essentially the same forward voltage of 0.65 to 0.75 V. However, the configuration shown in Figure 1-63(c) has speeds in the forward direction comparable to those of general-purpose computer diodes. When

using this configuration, care must be exercised to avoid exceeding the reverse breakdown of 6.0 V, mentioned earlier.

4. Comparison of Linear Circuit Design Philosophies

The preceding paragraphs have indicated that the performances of individual components and the obtainable component values and tolerances are certainly not comparable to those presently available in discrete components. However, for the design engineer who has established in his own mind a new linear-circuit design philosophy, the monolithic-microcircuit design constraints imposed on him are no worse than those imposed by the changeover from vacuum tubes to transistors.

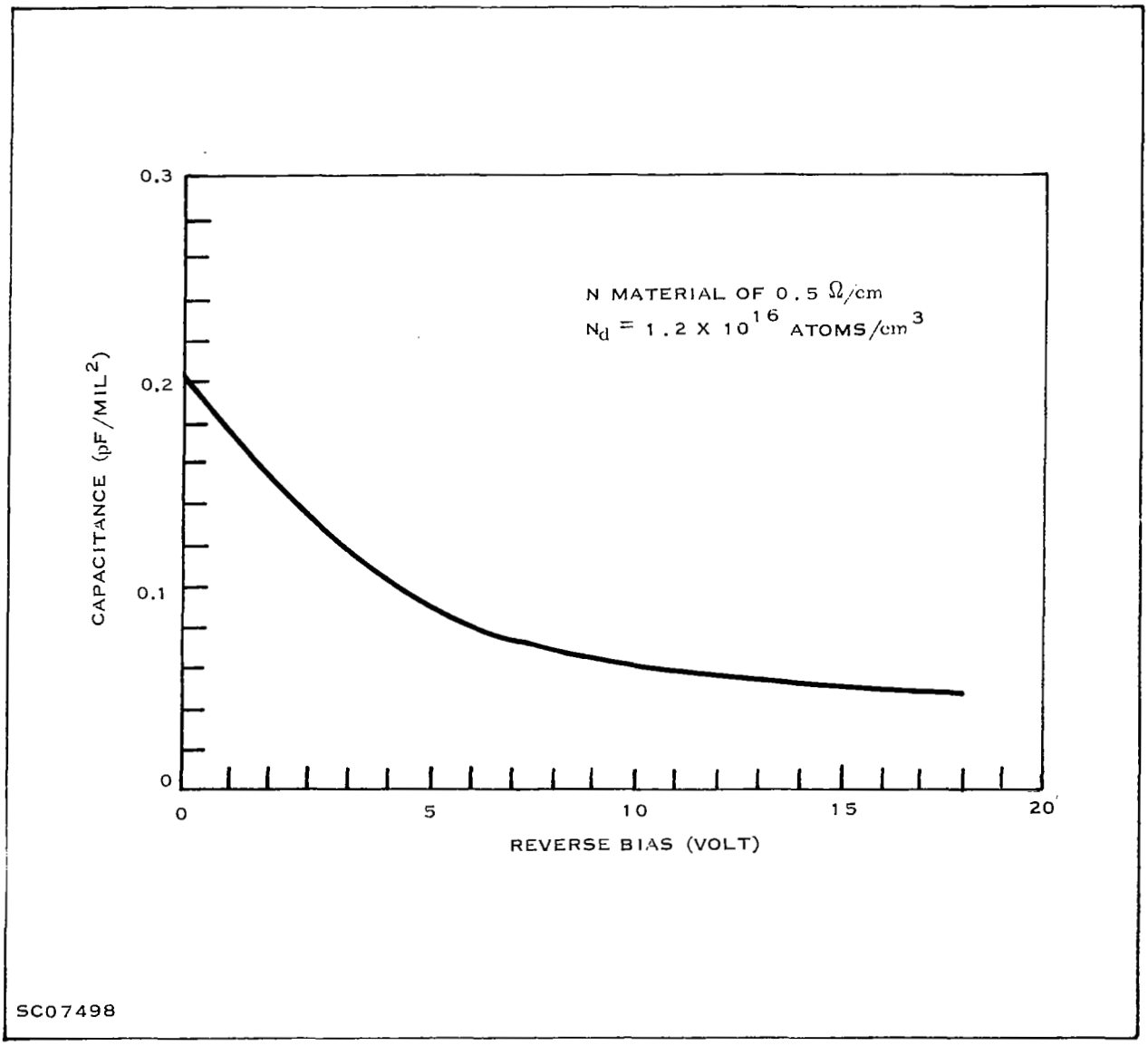
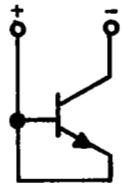
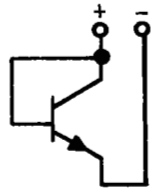


Figure 1-62. Relationship Between Diffused Capacitance and Reverse Bias Voltage

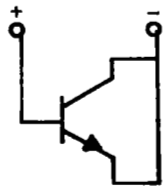
A. BASE TO COLLECTOR, WITH EMITTER OPEN



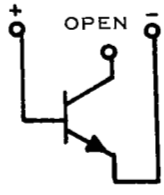
B. BASE TO COLLECTOR, WITH EMITTER SHORTED TO BASE



C. BASE TO EMITTER, WITH COLLECTOR SHORTED TO BASE



D. BASE TO COLLECTOR-EMITTER



E. BASE TO EMITTER, WITH COLLECTOR OPEN

SC07499

Figure 1-63. The Five Possible Diode Configurations Offered By The Diffused Transistor

The meaning of the term, "new linear-circuit design philosophy," is that the linear designer should keep certain objectives in mind when designing a monolithic microcircuit. Those objectives are presented in the following listing, along with the comparable items for discrete-component circuit design, where possible, to show the change in design philosophy:

Monolithic	Discrete
• Design, utilizing good resistor-ratio tolerance and temperature-tracking rather than absolute resistive values.	• Design with close tolerance, low-temperature-coefficient resistors, since there is no correlation between different resistors.
• Design, utilizing to the greatest advantage the inherently matched transistors.	• Design so that there will be no need for matched transistors, if possible.
• Design without capacitors whenever possible by using transistors freely, since transistors are low in cost.	• Design, using capacitors freely if it will reduce the need for transistors, since transistors are the cost determining element.
• Design the resistors and transistors to have as little parasitic capacitance as possible.	• Not applicable.
• Design with only NPN's, when possible.	• Not applicable.

5. Other Advantages of Linear Microcircuits Over Discrete Designs

a. General

Linear circuits designed in monolithic form very often have several distinct advantages over a similar design using discrete components. These advantages are size, reliability, cost, and performance. Generally, these would all occur at the same time. However, quite often just one of these advantages may be sufficiently significant to make any slight disadvantage in one of the other three easily tolerable. For example, special designs for space applications initially may cost more than a discrete component design, but the reliability and size improvements justify their use.

The first three of these items will be covered very briefly, since they are covered in greater detail elsewhere in the Handbook and are equally applicable to either linear design or to digital design.

b. Size

In years past, the most talked about advantage of monolithic microcircuits was the tremendous reduction in size. However, as the technology has progressed, the reliability and cost are receiving greater and greater attention. A linear differential amplifier similar to the SN526 consumes, in packaged form, less than 0.006 cubic inches, while the discrete counterpart would require, even with a tight packing density, at least 1 cubic inch. This represents a volume reduction of at least 200 to 1, which is certainly significant. Examples of particular reductions in system volume and weight could be given but the size-weight advantage is rarely an argued point.

c. Reliability

The reliability of monolithic linear microcircuits is not yet as well determined as it is for digital microcircuits, due to the relative infancy of linear microcircuits. However, since linear microcircuits use the same processes, packages, and techniques, it is expected that their reliability will not be significantly different from that of digital microcircuits. Life tests and field data to date support this assumption. System improvements in the mean-time-between-failures (MTBF) figure—from 10 to 50 times better than that of a discrete-component system—have been reported. These improvements are due to the fact that almost all of the interconnections are internal to the package. These interconnections are fabricated by a well-controlled process and are not nearly so subject to failure as are the interconnections of discrete components, where every element has at least two man-made connections. In addition, this reliability increase is achieved through the packaging of the entire circuit within a hermetically sealed enclosure of small mass, which makes the circuit very immune to shock, vibration, humidity, etc.

d. Cost

Linear monolithic microcircuits are, in general, less costly than their discrete component counterpart, due to the fact that many humdreds of identical circuits are fabricated at the same time under a highly automated system. As shown in Figure 1-64, the cost of typical linear microcircuits has decreased steadily over the past few years due to technological advances.

6. Tricks in Monolithic Linear Design

Innovative circuit design is, in most cases, the only way to get around the microcircuit design constraints that were mentioned earlier. To offset the handicap of having to design linear circuits with components that have wide tolerances, the designer should take full advantage of the close parameter correlation brought about by all the circuit elements being produced simultaneously in one integrated chip. For

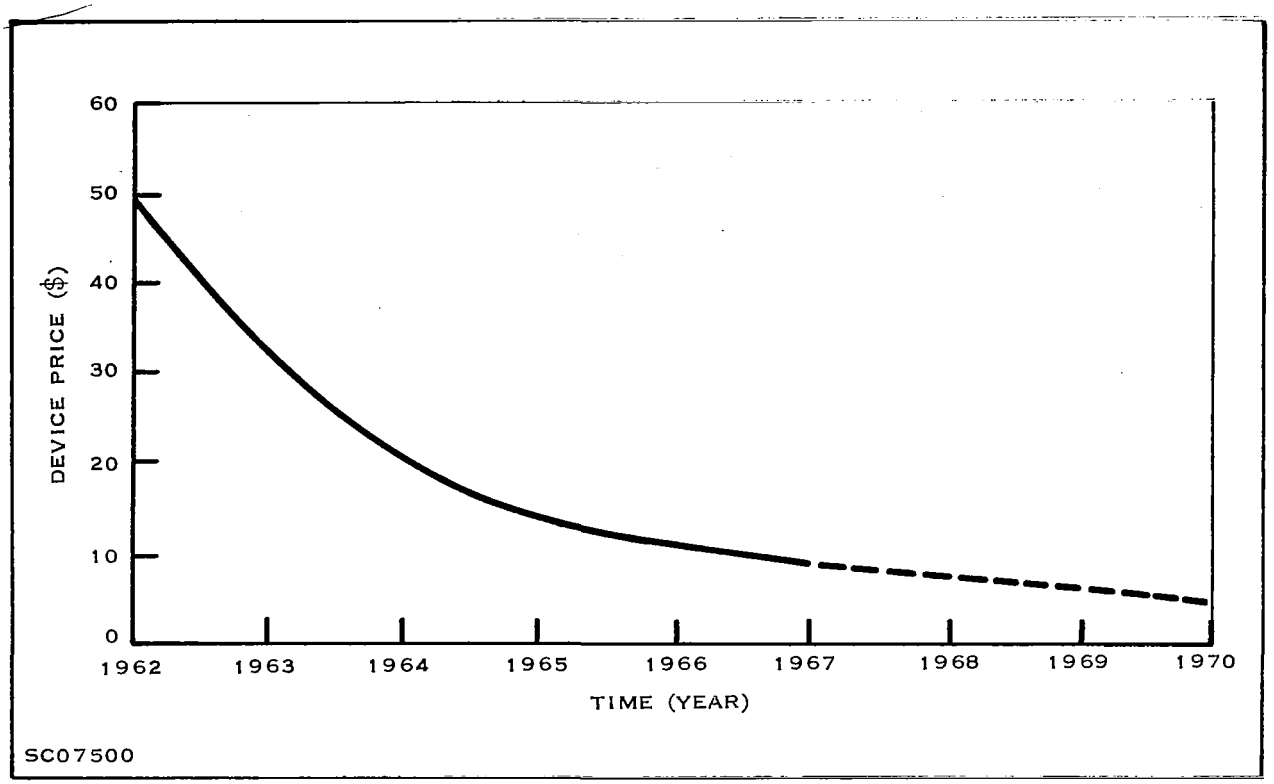
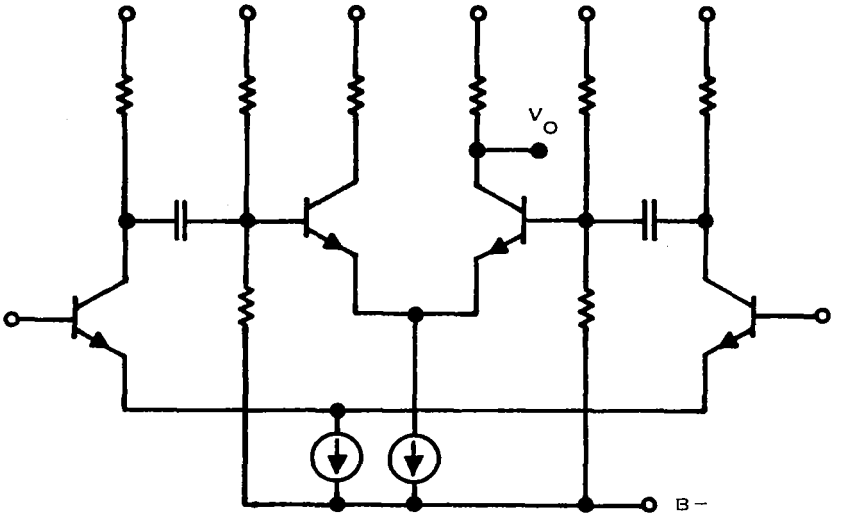


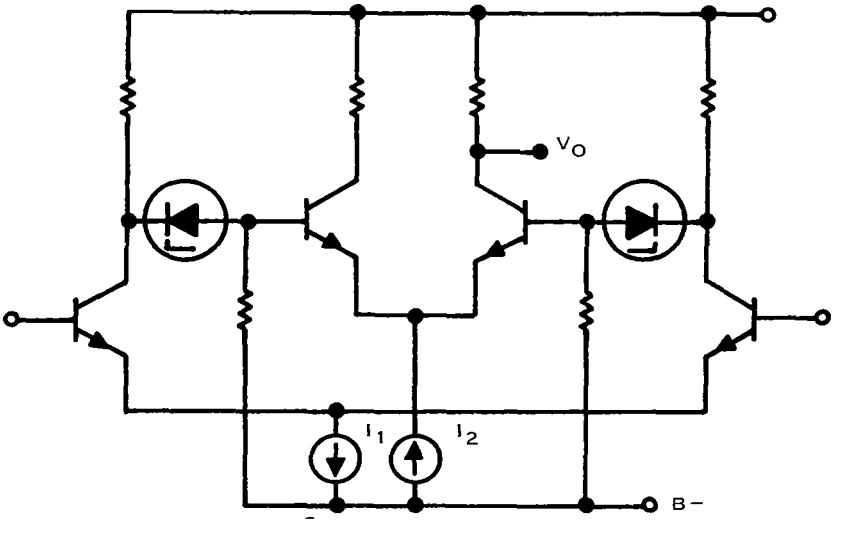
Figure 1-64 Decrease in Cost of Typical Linear Microcircuits Due to Technological Advances

example, very accurate resistive attenuators can be built from monolithic resistors even though such wide initial tolerances and extreme temperature coefficients exist. In addition, on a monolithic chip, a circuit designer essentially has a matched set of transistors at his disposal rather than having to choose them from large numbers of separate transistors, as in the discrete case. These well-matched transistors and the lack of reasonably sized coupling capacitors are the reasons most linear microcircuits are designed in a differential configuration.

It should be pointed out that complementary transistors on the same chip are possible but not desirable, since this generally requires a compromise in the device designs. Consider now, designing a differential, multistaged amplifier, using only NPN transistors. It is immediately recognized that, as one goes from stage to stage the collector bias levels are constantly rising towards B^+, since ac coupling is not possible, thereby restricting the output collector swing. A technique for getting around this problem, one that would be extremely difficult, if not impossible, to use with discrete components, is shown in Figure 1-65. Following the first stage, the bias level is shifted down through two matched zener diodes such that the resultant output dc level is the same as the input dc level, even though only NPN transistors and no coupling capacitors were used. These zener diodes will be matched on the chip to within 50 mV and will track almost identically over temperature. It would be very



(A) DISCRETE COMPONENT METHOD FOR LEVEL TRANSLATION



(B) MONOLITHIC MICROCIRCUIT METHOD FOR LEVEL TRANSLATION

SC07501

Figure 1-65 Discrete versus Monolithic Linear Circuit

difficult to find two discrete-component zener diodes that would match in voltage and temperature coefficients and could be used in such a manner.

Suppose a single-stage, common-emitter amplifier with maximum gain, as in Figure 1-66 is desired. The problem immediately recognized is that the emitter by-pass capacitor will not be available on the chip. Therefore, this capacitor must be placed outside the package and connected externally, or some other design innovation must be found, as in Figure 1-66. Here, a second transistor, biased "on," is used to form the low ac impedance seen from the first emitter. This does a good job of bypassing the first-stage emitter resistor to allow the total possible gain of the transistor, as long as the betas are reasonable.

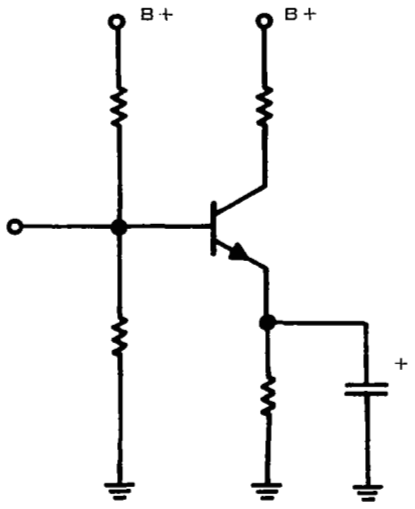
Fortunately, a number of the so-called disadvantages of microcircuits may be turned on themselves and utilized to the designer's advantage. In fact, even the parasitic capacitances may be employed as useful circuit elements. The phase shift oscillator shown in Figure 1-67 uses the distributed capacitance associated with diffused resistors to form the phase shift network. Applications such as this are limited only by the designer's imagination and knowledge of the component characteristics.

The linear microcircuit designer has a very important tool at his disposal by which he can design around some of the constraints mentioned. This tool is the ability to vary the geometry of transistors and resistors to achieve the particular component characteristics that are desired.

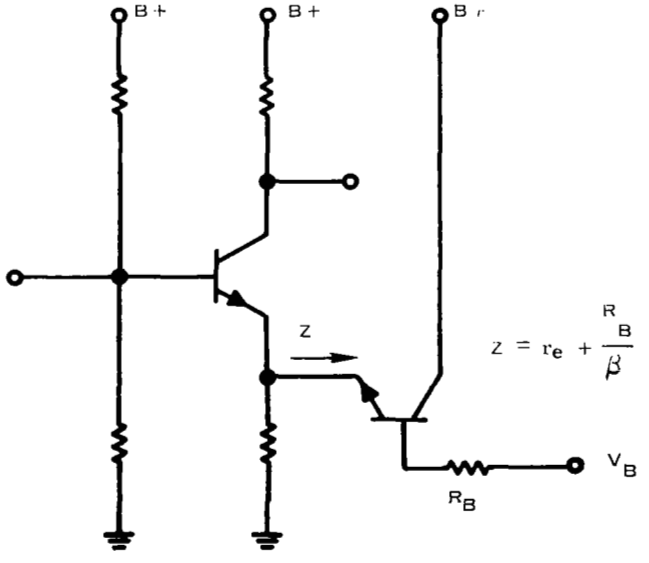
7. Summary

This discussion has brought out the fact that monolithic microcircuit components, taken one at a time, are admittedly less desirable for design purposes than are the discrete components available today. However, when the "monolithic versus discrete linear" case is argued on a circuit-function basis, the monolithic design is, in most cases, comparable to the discrete design in performance, and sometimes is better. One example would be the case when matched components and components that will track well over temperature are a primary part of the design. Of course, when the case is argued from a size or reliability standpoint, there can be no doubt that the monolithic microcircuit offers an extreme advantage. Therefore, when the advantages and disadvantages of the linear monolithic microcircuit are clearly understood and acknowledged, one must admit that monolithic technology does indeed lend itself to the design of linear circuits that can, in most small-signal cases, offer more of an overall advantage than the identical circuit designed from discrete components.

For frequencies in excess of 100 MHz, the totally monolithic circuit may not be sufficient. Such an application may require a hybrid combination of the thin film and monolithic technologies; however, this is outside the scope of this Handbook.



(A) DISCRETE HIGH-GAIN SINGLE-STAGE AMPLIFIER WITH EMITTER BYPASS CAPACITOR



(B) MONOLITHIC MICROCIRCUIT HIGH-GAIN AMPLIFIER WITH CAPACITOR REPLACED BY TRANSISTOR STAGE

SC07502

Figure 1-66. Discrete versus Monolithic High-Gain Stage

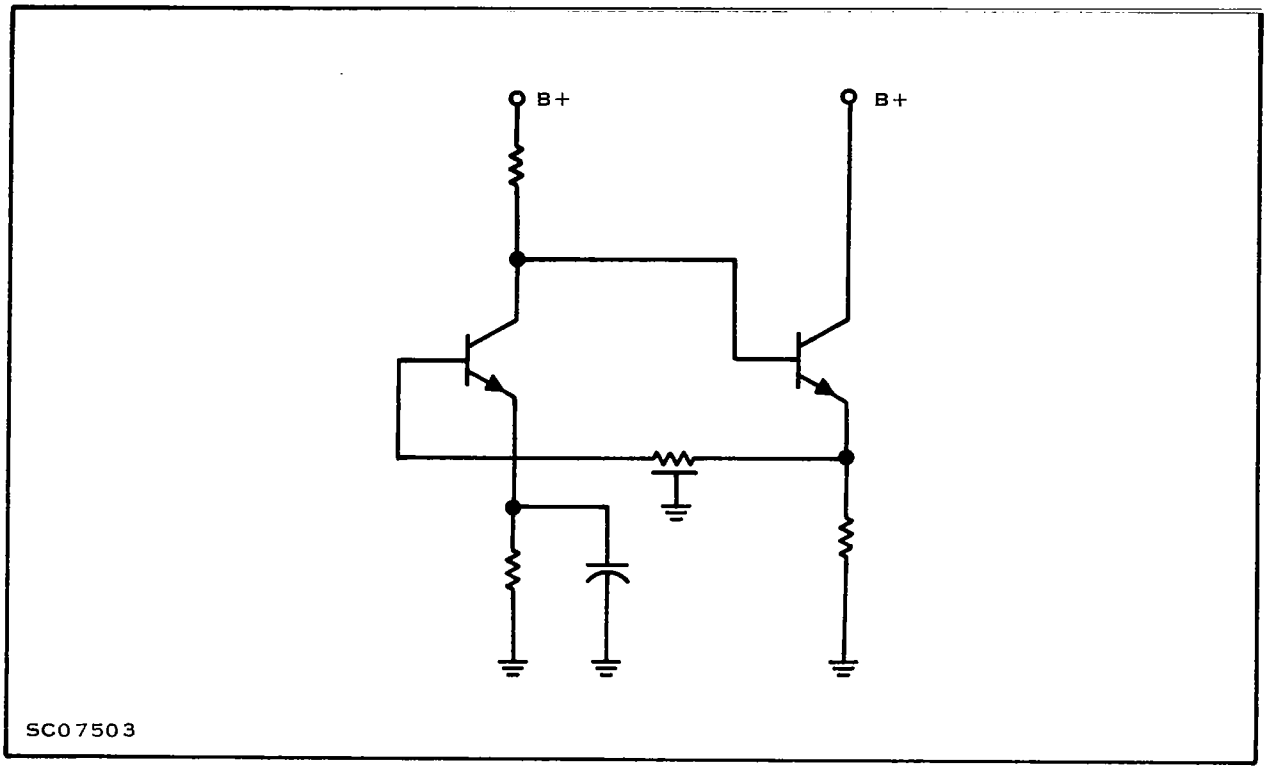


Figure 1-67. A Phase Shift Oscillator That Uses The Distributed Parasitic Capacitance of Diffused Resistors to Form Its Phase Shift Network

B. DEFINITIONS OF LINEAR TERMS AND PARAMETERS

1. General

The purpose of this discussion is to define and discuss the terms and parameters most commonly used in the discussion and specification of linear microcircuits. Only those terms and parameters that apply to operational amplifiers, differential amplifiers and differential comparators will be presented. A basic understanding of these definitions is necessary before proceding with the discussion of examples and analyses of linear circuits, since circuit terms and parameters will be freely used without explanation. A clear understanding of these definitions will also allow the reader to extract the maximum amount of information from a data sheet.

Since little has been done, to date, toward standardizing the definitions and symbols that will be presented here, the reader may find differences when comparing separate sources. In general, these differences will be minor and noncontradictory. Standard EIA procedures will be followed whenever possible.

2. Operational Amplifiers

The term "operational amplifier," when used in a monolithic microcircuit discussion, has acquired a somewhat different meaning than the literal definition. An ideal operational amplifier is defined as one that has infinte gain and input impedance, zero-offset voltage and output impedance, differential input, and single-ended output. The fact that no amplifier can possibly meet this definition has led to considerable confusion as to what is required of an amplifier so that it may be called "operational."

Common and accepted usage of the term "operational amplifier" in the monolithic-microcircuit industry has come to mean an amplifier with differential input, single-ended output, gain in excess of 60 dB, and an input impedance of at least 100 kΩ. Admittedly, this definition is neither standardized nor universally accepted. However, it is a reasonable definition and will be used here.

3. Differential Amplifiers

A differential amplifier is one that has differential output as well as differential input. The definition places no restriction whatsoever on gain, impedance levels, or bandwidth. Obviously, if a differential amplifier has high gain and input impedance, it can be operated using only one of the outputs, in which case it could be termed an operational amplifier. However, we will abide by the definition that if a differential output exists, it will be called a differential amplifier.

4. Differential Comparators

A differential voltage comparator is similar to an operational amplifier in that it has a differential input, single-ended output, and high gain. However, the output of a differential comparator is a digital signal that is either "high" or "low," depending on which input is higher than the other. Operational amplifiers can be used to perform a comparator function but will not recover from saturation as fast as a true comparator. In addition, a true comparator generally has a lower output swing, to be compatible with low-level logic circuits.

5. Inverting and Noninverting Inputs

The terms "inverting input" and "noninverting input" are reasonably self-explanatory. However, due to their importance and occurrence in this discussion, their definitions are included. When speaking in terms of an operational amplifier, i.e., single output, or one particular output of a differential amplifier, the noninverting input is that input that is in phase with the output. The inverting input's definition is the converse. One uses the noninverting input when closing positive feedback around an amplifier, and the inverting input is used for negative feedback.

6. Definitions of Data Sheet Items and Parameters

a. General

Many of the data-sheet items and parameters to be defined are applicable to all three devices under discussion, i.e., comparators, operational amplifiers, and differential amplifiers, while others are either applicable to only one of the three device types or at least require a special definition. Therefore, the method of approach will be, first, to define those items applicable to all three, and then to proceed to those items that pertain to each individual device type.

b. Definitions Pertaining to Operational Amplifiers, Differential Amplifiers, and Comparators

The absolute maximum limits of current, voltage and temperature for operational amplifiers, differential amplifiers, and comparators are symbolized and defined in Table 1-9.

Table 1-9. Absolute Maximum Current, Voltage, and Temperature for Operational Amplifiers, Differential Amplifiers and Comparators

Parameter	Symbol	Definition
Maximum Positive Supply Voltage	V_{CC}, V_{CC^+}	That voltage which, if exceeded, may cause permanent damage to the device.
Maximum Negative Supply Voltage	V_{CC}, V_{CC^-}	That voltage which, if exceeded, may cause permanent damage to the device.
Maximum Total Supply Input Voltage		The total difference in voltage between the two input terminals that must not be exceeded for predictable operation.
Maximum Input Voltage	V_{in}	That voltage at either input terminal that may cause permanent damage if exceeded.
Peak Load Current	I_L	The maximum current that can be supplied to the load without probable permanent damage.
Maximum Lead Temperature		The maximum lead temperature allowed for a specified length of time during a soldering or welding process, to insure no internal damage.

Table 1-9. Absolute Maximum Current, Voltage, and Temperature for Operational Amplifiers, Differential Amplifiers and Comparators (continued)

Parameter	Symbol	Definition
Storage Temperature Range	T_{stg}	The range of temperature at which the device may be stored, retaining its capability to operate properly and reliably when removed from storage.
Operating Temperature Range	T_A	The range in case-temperature over which the device may be operated and still function within specifications.

Power-supply parameters, their symbols and definitions, for operational amplifiers, differential amplifiers and comparators, are shown in Table 1-10.

Table 1-10. Power Supply Parameters for Operational Amplifiers, Differential Amplifiers and Comparators

Parameter	Symbol	Definition
Total dc Power Dissipation	P_T, P_D	The total power drain of the device with no signal applied and with no load current.
Total Power Dissipation Derating Factor		A factor given in milliwatts per degree C to apply to the maximum allowed power dissipation when operating at case-temperatures above a specified temperature.
Supply Voltage Rejection Ratio		The ratio of the change in input offset voltage to the change in supply voltage.

The symbols and definitions for the static input parameters are presented in Table 1-11.

Table 1-11. Static Input Parameters for Operational Amplifiers, Differential Amplifiers and Comparators

Parameter	Symbol	Definition
Input Offset Voltage Temperature Coefficient	α_{VDI}, TC_{VD}	The ratio of the change in input offset-voltage to a specified change in temperature.
Input Bias Current	I_{in}	The average of the two currents into the input terminals.

c. Definitions Pertaining To Operational Amplifiers (Defined as Having A Single Output)

The static input parameters of operational amplifiers are presented in Table 1-12, and the synamic parameters are shown in Table 1-13.

Table 1-12. Static Input Parameters of an Operational Amplifier

Parameter	Symbol	Definition
Differential Input Offset Voltage	V_{DI}, V_{DIO}	That dc voltage which must be applied between the input terminals to obtain zero output voltage.
Differential Input Offset Current	I_{DI}, I_{DIO}	The difference in the currents into the two input terminals when the output is at zero volts.

Table 1-13. Dynamic Parameters of an Operational Amplifier

Parameter	Symbol	Definition
Open-loop Voltage Gain	A_V, A_{VOL} A_{OL}	The ratio of the change in output voltage to the change in voltage between the input terminals producing it.
Large-signal Voltage Gain		The ratio of the maximum output voltage swing into a specified load to the input voltage to obtain maximum output voltage.
Open-loop Bandwidth	BW, BW_{OL}	The frequency at which the voltage gain of the device is 3 dB below the voltage gain at a specified lower frequency.
Input Impedance (r_{in} is sometimes referred to as input resistance.)	Z_{in} r_{in}	The ratio of the change in input voltage to the change in input current, measured at either input terminal with respect to ground, with the other input terminal ac-grounded and the amplifier connected open loop.
Output Impedance (r_{out} is sometimes referred to as output resistance.)	Z_{out} r_{out}	The ratio of the change in output voltage to the change in output current, measured with respect to ground at the output terminal, with the output at a null condition.

Table 1-13. Dynamic Parameters of an Operational Amplifier (continued)

Parameter	Symbol	Definition
Common-mode Input Voltage Limit	V_{CML}	The peak voltage that can be applied to both input terminals without saturating the output.
Output Voltage Swing	V_{out}	The peak output swing referred to zero that can be obtained without clipping into a specified load.
Common-mode Rejection Ratio	CMRR	The ratio of the change in output voltage to the change in input common mode voltage producing it, divided by the open-loop voltage gain.
Input Noise Voltage	$V_{N(in)}$	The rms value of the output noise voltage, into a specified load and at a specified bandwidth, divided by the open-loop voltage gain.

d. Definitions Pertaining to Differential Amplifiers

For the static input parameters and the dynamic parameters of differential amplifiers, see Table 1-14 and 1-15, respectively.

Table 1-14. Static Input Parameters of a Differential Amplifier

Parameter	Symbol	Definition
Differential Input Offset Voltage	V_{DI}, V_{DIO}	That dc voltage which must be applied between terminals to obtain zero differential output voltage. The application of this voltage balances the amplifier.
Differential Input Offset Current	I_{DI}, I_{DIO}	The difference in the currents into the two input terminals when the two outputs are balanced.

Table 1-15. Dynamic Parameters of a Differential Amplifier

Parameter	Symbol	Definition
Single-ended Open-loop Voltage Gain	A_V, A_{VSO}	The ratio of change in the single-ended output voltage to a change in the differential input voltage.
Differential Open-loop Voltage Gain	A_V, A_{VDO}	The ratio change in the differential output voltage to the change in the differential input voltage. This differential voltage gain is twice the single-ended voltage gain.
Open-loop Bandwidth	BW, BW_{OL}	The frequency at which the voltage gain of the device is 3 dB below the voltage gain at a specified lower frequency.
Input Impedance (r_{in} is sometimes referred to as input resistance)	Z_{in} r_{in}	The ratio of the change in input voltage to the change in input current, measured between either input terminal and ground with the other input terminal ac-grounded and the outputs balanced.
Output Impedance (r_{out} is sometimes referred to as input resistance)	Z_{out} r_{out}	The ratio of the change in output voltage to the change in output current, measured between either output terminal and ground when the outputs are balanced.
Common-mode Input Voltage Limit	V_{CMI}	The peak voltage that can be applied to both input terminals without saturating either output.
Maximum Output Voltage Swing	V_{OM}, V_{out}	The maximum peak-to-peak output swing that can be obtained without clipping at either output when the outputs are balanced.
Common-mode Rejection Ratio	CMRR	The ratio of the common-mode input voltage of the single-ended common-mode output voltage referenced to the input.
Input Noise Voltage	$V_{N(in)}$	The rms value of the output noise voltage into a specified load at a specified bandwidth, divided by the single-ended voltage gain.

Table 1-15. Dynamic Parameters of a Differential Amplifier (continued)

Parameter	Symbol	Definition
Noise Figure	NF	The ratio of the total noise power of the device and a resistive signal source, to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with a source resistance.
Common-mode Offset Voltage	V_{CMO}	The dc voltage level that exists between the output terminals and ground when the outputs are balanced.
Total Harmonic Distortion	THD	The ratio, expressed as a percent, of the total rms voltage of all signal harmonics at either output terminal to the rms voltage of the fundamental.
AGC Range	AGC	The total change in voltage gain produced by varying a dc voltage to the AGC input terminal of the device, if the device possesses such capability.

e. Definitions Pertaining to Differential Comparators

The static input parameters and the dynamic parameters of a differential comparator are shown in Tables 1-16 and 1-17, respectively.

Table 1-16. Static Input Parameters of a Differential Comparator

Parameter	Symbol	Definition
Differential Input Threshold Voltage	V_T	The pulse or dc input voltage that is just sufficient to cause the output to switch.
Differential Input Offset Voltage	V_{DI}, V_{DIO}	The voltage between the input terminals when the output is at the logic-threshold voltage.
Differential Input Offset Current	I_{DI}, I_{DIO}	The difference in the currents into the two input terminals with the output at the logic-threshold voltage.

Table 1-17. Dynamic Parameters of a Differential Comparator

Parameter	Symbol	Definition
Voltage Gain	A_V	The ratio of the change in output voltage to the change in differential input voltage with the dc output level in the vicinity of the logic threshold voltage.
Output Impedance (r_{out} is sometimes referred to as output resistance)	Z_{out} r_{out}	Ratio of the change in output voltage to the change in output current at the output terminal, with the dc output level at the logic threshold voltage.
Differential Input Voltage Range	V_{in}	The maximum voltage between the two input terminals for which operation within specifications is assured.
Logical "1" Output Voltage	$V_{out("1")}$	The dc output voltage in the positive direction, with the input voltage equal to or greater than a specified minimum amount.
Logical "0" Output Voltage	$V_{out("0")}$	The dc output voltage in the negative direction, with the input voltage equal to or greater than a minimum amount.
Response Time		The time delay between the application of a step function to the input and the time when the output reaches the logic threshold voltage.
Strobed Output Level		The dc output voltage, with the voltage on the strobe terminal (if one exists) equal to or less than a specified minimum amount.
Strobe Current	I_s	The maximum current drawn by the strobe input when it is at the zero logic level.
Strobe Release Time		The time required after the strobe terminal has been driven from the "zero" logic level to the "one" logic level, for the output to rise to the logic threshold voltage.

7. Summary

As previously mentioned, very little has been accomplished in standardizing the definitons and symbols given in the preceding paragraphs. As a result, data sheets on linear microcircuit devices will vary from manufacturer to manufacturer, and sometimes from one device to another from the same manufacturer. Most of the parameters defined here must have certain test conditons specified, such as the load, temperature, source impedance, etc. Some data sheets are very incomplete in that graphical representations of some of the parameters are presented as a function of a particular test condition.

In conclusion, since all of the parameters defined in this discussion are seldom specified on any one device, it is very important to understand completely the parameters and test conditions that are specified in order to obtain as much information from the data sheet as possible.

C. EXAMPLES AND ANALYSES OF LINEAR CIRCUITS

1. General

To permit better understanding of the operation of monolithic linear microcircuits, a typical example of each type has been chosen for analysis and discussion. The function of each element in the circuit, and possible variations in performance due to temperature, loading, power supply variation, etc., will be discussed for each example. Detailed design equations will be avoided, in general, but may be used whenever necessary to make a particular point clear. The intent is that the reader be able to apply these discussions and principles to other available comparators and amplifiers which, in principle, are very similar to those discussed here. The circuits chosen as examples of monolithic linear microcircuits are as follows:

Operational-Differential Amplifier	SN526	Texas Instruments
Differential Amplifier	CA3000	RCA
Differential Comparator	μA711	Fairchild

These are the same networks discussed previously for data-sheet representation, and they are presented here to maintain continuity throughout this discussion of linear microcircuits. The choices are not intended to imply recommendation or preference in any way for either the manufacturer or the device type. It should also be noted that several manufacturers other than those mentioned may have these devices available.

2. Operational - Differential Amplifier (SN526, (Texas Instruments)

a. General

The SN526 linear monolithic amplifier package contains a differential input, differential output amplifier and a Class B, single-ended input, single-ended output, power amplifier. In other words, there is a differential amplifier and a single-ended Class B amplifier independently contained in the same package. The input to the Class B amplifier may be connected to either output of the differential amplifier, or left unconnected. Therefore, the SN526 can be discussed as either a differential amplifier (Class B disconnected) or as an operational amplifier (Class B connected). The approach here will be to discuss the differential amplifier portion first, neglecting the Class B stage, and then to discusss the Class B stage.

b. Differential Amplifier Portion

The differential amplifier portion of the SN526, as shown in Figure 1-68 contains two cascaded gain stages and a common-mode feedback amplifier.

The input stage is composed of transistors Q_1, Q_2, Q_3 and Q_4, which form two modified Darlington input pairs. Transistor Q_7 acts as a current source for the first stage. This current source is also a part of the common-mode feedback mechanism and will be explained later. A simplified version of the first stage is shown in Figure 1-69.

The modified Darlington inputs result in an input impedance that has a small reactive component and a large real component. Reference to the data sheet shows this to be 2 MΩ, typically. Therefore, high input impedance is achieved without compromising the overall bandwidth characteristic. An ordinary Darlington connection, as shown in Figure 1-70(a), results in a high input capacity due to the large voltage gain between the collector and base of the first transistor. However, the modified Darlington, as shown in Figure 1-70(b), does not have this problem, due to the fact that the collectors of Q_1 and Q_2 are at ac ground when they are driven differentially. These collectors, being at ac ground, result in zero voltage gain between the collector and base of Q_1 and Q_2; therefore the Miller Multiplication effect has been eliminated.

The input bias currents are made very small by such a connection, because Q_1 and Q_2 only have to supply base current to Q_3 and Q_4. In other words, a high dc current gain exists in such an input stage. The data sheet specifies the input bias current to be 100 μA, typically.

At the same time, however, the differential input offset voltage is worse than if only single transistors were used on each side of the input stage. Input

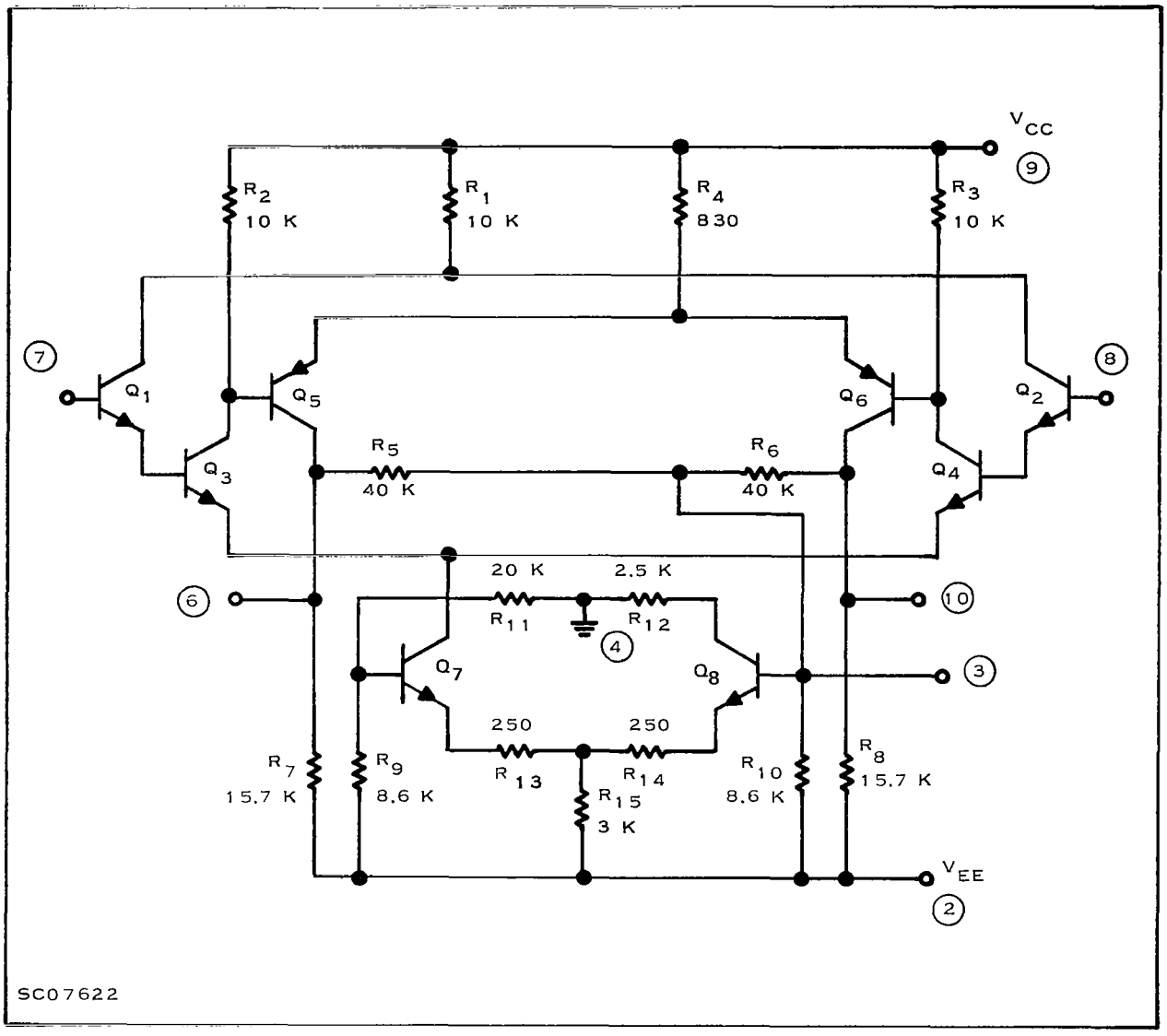


Figure 1-68. Differential Portion of Operational-Differential Amplifier (SN526, Texas Instruments)

offset voltage is, in reality, a function, or measure, of the match in the input-transistor V_{be}'s on the two sides. It is, therefore, obvious that since the input stage under discussion has two transistors on either side instead of one, the total possible V_{be} mismatch between the two sides will be approximately twice as much as in the single transistor case. The data sheet shows the differential input offset voltage to be 3 mV, typically. The same basic argument applies to the input bias offset current (30 nA) and the differential input offset voltage temperature coefficient (15 μV/°C), in that the matching and temperature tracking on the two sides is half as good as in a normal input situation.

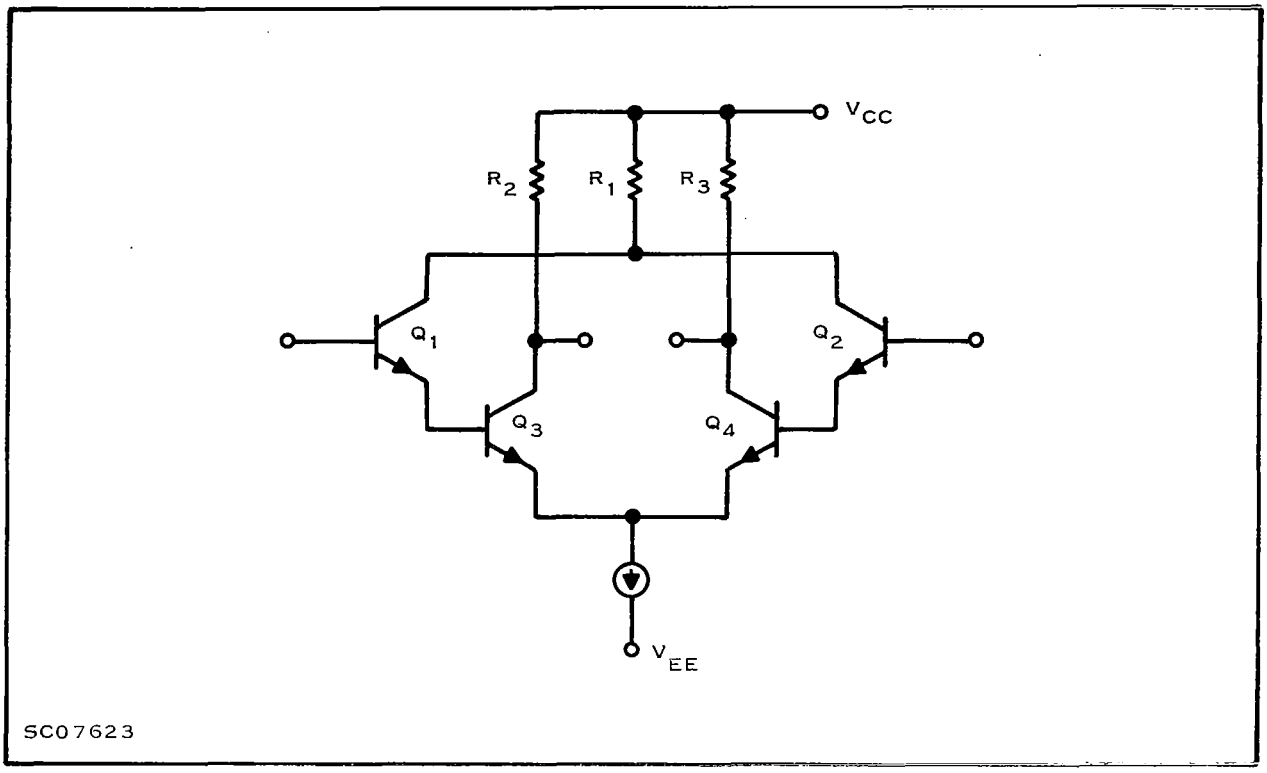


Figure 1-69. Simplified Version of First Stage of SN526

The current source, Q_7, allows the first-stage current to be relatively insensitive to common-mode variations in the input dc voltage. Therefore, the input stage is completely capable of accepting either positive or negative common-mode signals, i.e., signals common (in phase) to both inputs.

The second gain-stage consists of Q_5 and Q_6, which form a differential pair of PNP transistors that are driven by the first stage. The second stage is shown in simplified form in Figure 1-71. The collector voltages of Q_3 and Q_4, and hence the emitter voltages of Q_5 and Q_6, form a dc voltage across R_4, which then acts as the current source for the second stage.

If we now consider the first and second stages together, as in Figure 1-68, and assume a differential input signal between pins 7 and 8, the signal will be inverted and amplified to the collectors of Q_3 and Q_4. This differential signal at the bases of Q_5 and Q_6 will then be amplified and inverted once again before appearing at the collectors of Q_5 and Q_6, which are the outputs.

The common-mode feedback amplifier consists of Q_7, Q_8, and associated resistors, as shown isolated in Figure 1-72. It should be mentioned again here, that in this instance, the discussion will be in terms of common-mode signals, i.e., a signal common to both sides, whether ac or dc. Suppose, for example, that

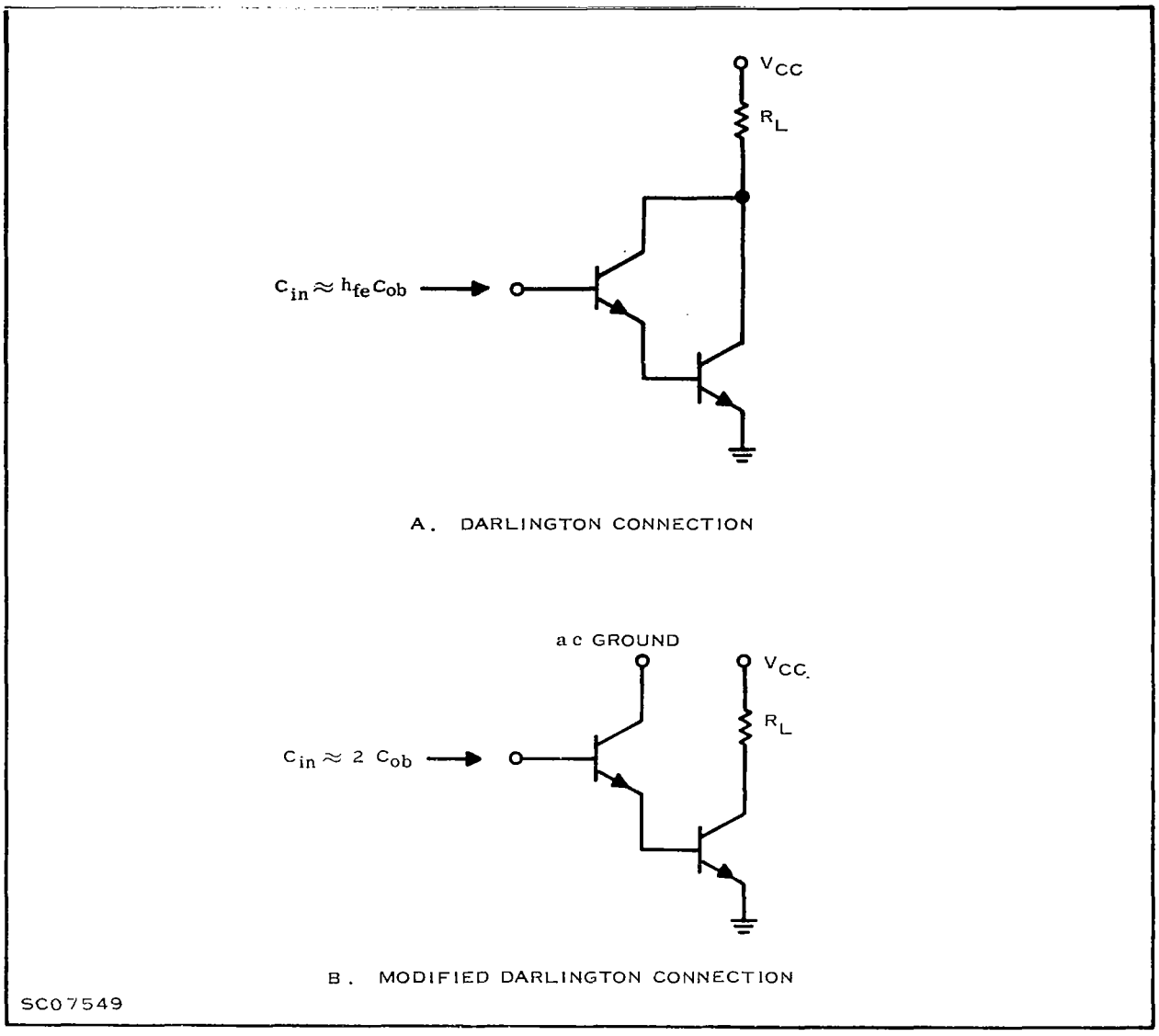


Figure 1-70. Darlington-Input Pair from First Stage of SN526

in Figure 1-68 the outputs (pins 6 and 10) are attempting to rise, common mode. This will cause points A and B in Figure 1-72 to rise. When this happens, the bias voltage on the base of Q_8 rises, causing more current to flow in Q_8 and less in Q_7, since Q_7 and Q_8 are connected differentially. This will cause the voltages on the bases of Q_5 and Q_6 in Figure 1-68 to rise, since less current is being pulled through R_2 and R_3. This will, in turn, tend to turn Q_5 and Q_6 "off," which will result in a lowering of the voltages at the output pins, which, you will remember, were attempting to rise. Hence, common-mode feedback exists for rejection of common-mode signals and stabilization of the output dc level. These common-mode signals could be signals appearing on the inputs or effective signals resulting from common changes in V_{be} and h_{fe} of the transistors as a function of temperature. Due to the high gain in the

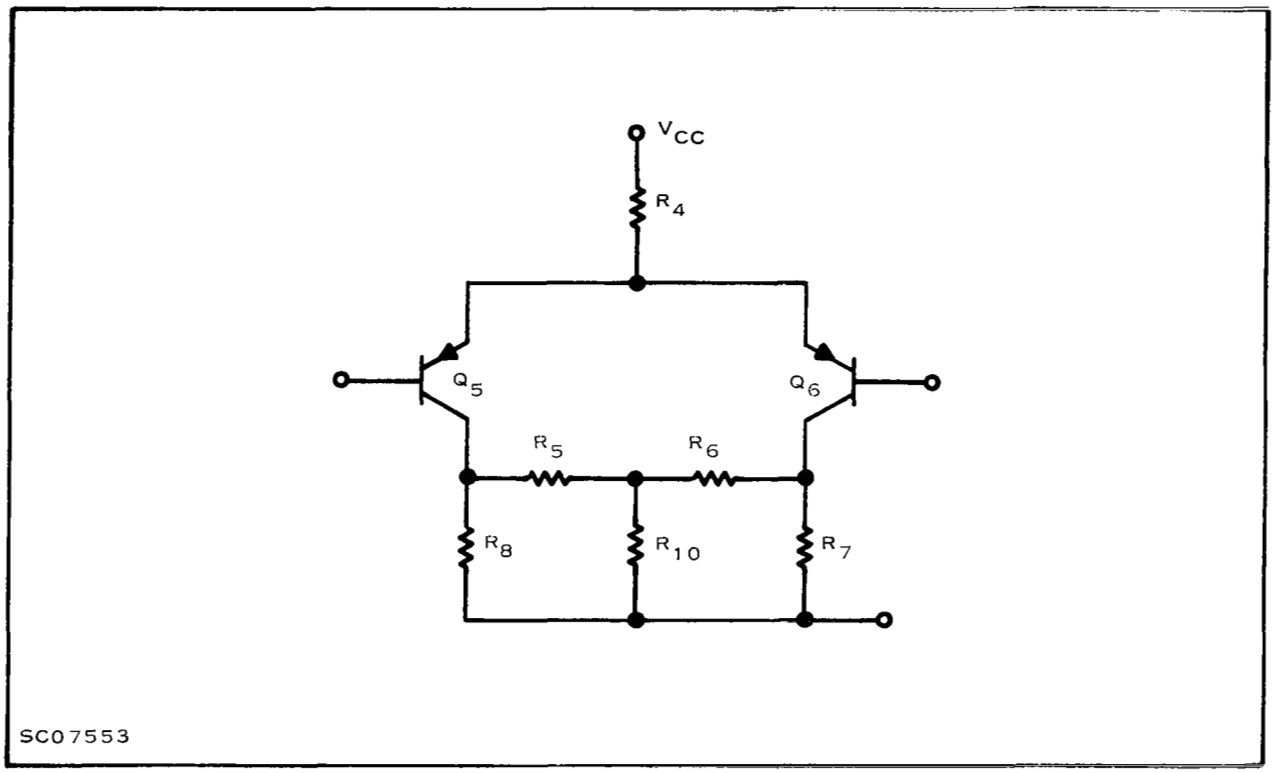


Figure 1-71. Second Stage of SN526

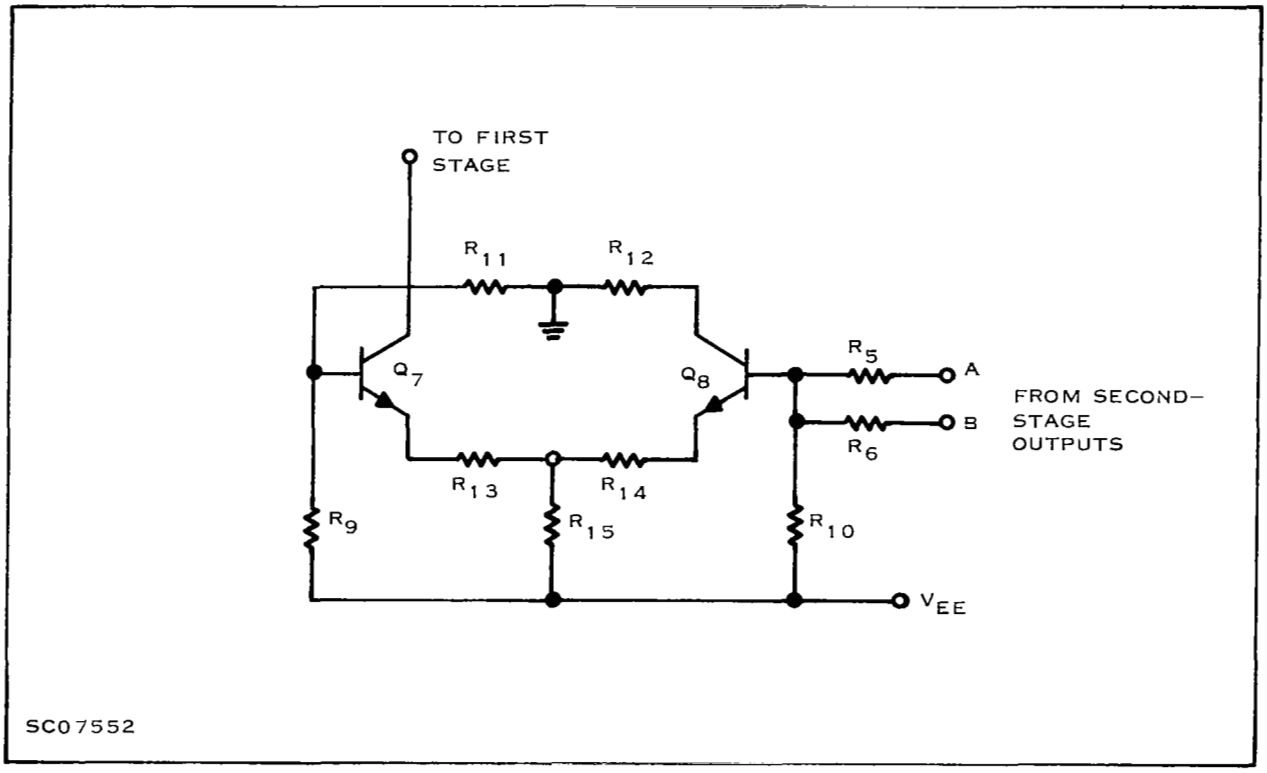


Figure 1-72. Common-Mode Feedback Amplifier of SN526

common-mode feedback loop, an external capacitor of 220 pF from pin 3 to ground is recommended for stabilizing the common-mode loop. The data sheet shows typical common-mode rejection of 80 dB.

The differential gain equation for the first stage can be derived to be approximately:

$$A_1 \approx \frac{R_2 \beta_2 r_{e2}}{2r_{ei}(R_2 + \beta_2 r_{e2})} \tag{5}$$

where

β_2 = h_{fe} of Q_5 or Q_6

r_{e2} = Emitter resistance of Q_5 or Q_6

r_{e1} = Emitter resistance of Q_3 or Q_4

now

$$re = \frac{KT}{qI_e}$$

so

$$r_{ei} = 52$$

and

$$r_{e2} = 13$$

assuming

$$\beta_2 = 20$$

$$A_1 \approx 2.7$$

The differential voltage gain of the second stage can likewise be derived to be approximately:

$$A_2 \approx \frac{R_6 R_7}{r_{e2}(R_6 + R_7)} \tag{6}$$

$$A_2 \approx 860$$

Therefore, the total differential gain is $A_1 \cdot A_2$, or 2300, typically, which is in agreement with the data sheet.

The output impedance is approximately $R_6 \,||\, R_7$, or 12 kΩ. This means that it will be difficult to drive a very low impedance load. However, as the data sheet points out, 12 V_{p-p} is able to be driven single-ended into a 600-Ω load. In general, the load impedance will be greater than 600 Ω.

Temperature will cause only two variations worth considering. The first is the variation in differential input offset voltage, which the data sheet shows to be 15 μV/°C. This offset will appear at the outputs as having been amplified by the closed-loop gain. The second variation is a slight reduction in open-loop gain caused by the temperature term in r_e that appears in the gain equation. For most applications, sufficient negative feedback is applied to make both of these relatively insignificant.

Reduction in power supply voltage, if done unsymmetrically, will have only the effect of reducing the open-loop gain slightly due to changing the bias current I_e which appears in the gain equation.

c. Operational Amplifier Connection

As previously mentioned, when pin 5 is connected to pin 6 or 10, the result is a very good operational amplifier. In actuality, it is the differential amplifier just discussed, with one output connected to the input of a Class B power output stage. This output stage is shown in Figure 1-73. The purpose of such an output stage is to provide unity gain, high output voltage, and current ranges with small standby power and crossover distortion.

Transistors Q_{10} and Q_{11} have several functions: to bias and temperature-compensate Q_{12} and Q_{13}, act as drivers for Q_{12} and Q_{13}, and form a high-impedance load with respect to pin 5. Transistor Q_9 acts as a constant-current source for R_{19}. The dc voltage developed across R_{19} subtracts from the emitter-follower V_{be}'s, so that Q_{12} and Q_{13} will only be slightly "on." This maintains the standby power at a minimum. If this voltage across R_{19} were too large, Q_{12} and Q_{13} would be totally "off," and crossover distortion at the output would occur because it would take some amount of signal voltage input to the bases of Q_{12} or Q_{13} before they would turn "on." Crossover distortion is depicted in Figure 1-74.

As the input at pin 5 goes positive, Q_{10} is turned "on" with more certainty, which in turn creates a voltage across R_{20}, turning Q_{13} "off." Likewise, Q_{11} is being turned "off," which raises the voltage at the base of Q_{12}, turning it "on." Hence, current is being sunk by the load. For a negative input at pin 5, the reverse takes place and results in current being supplied by the load.

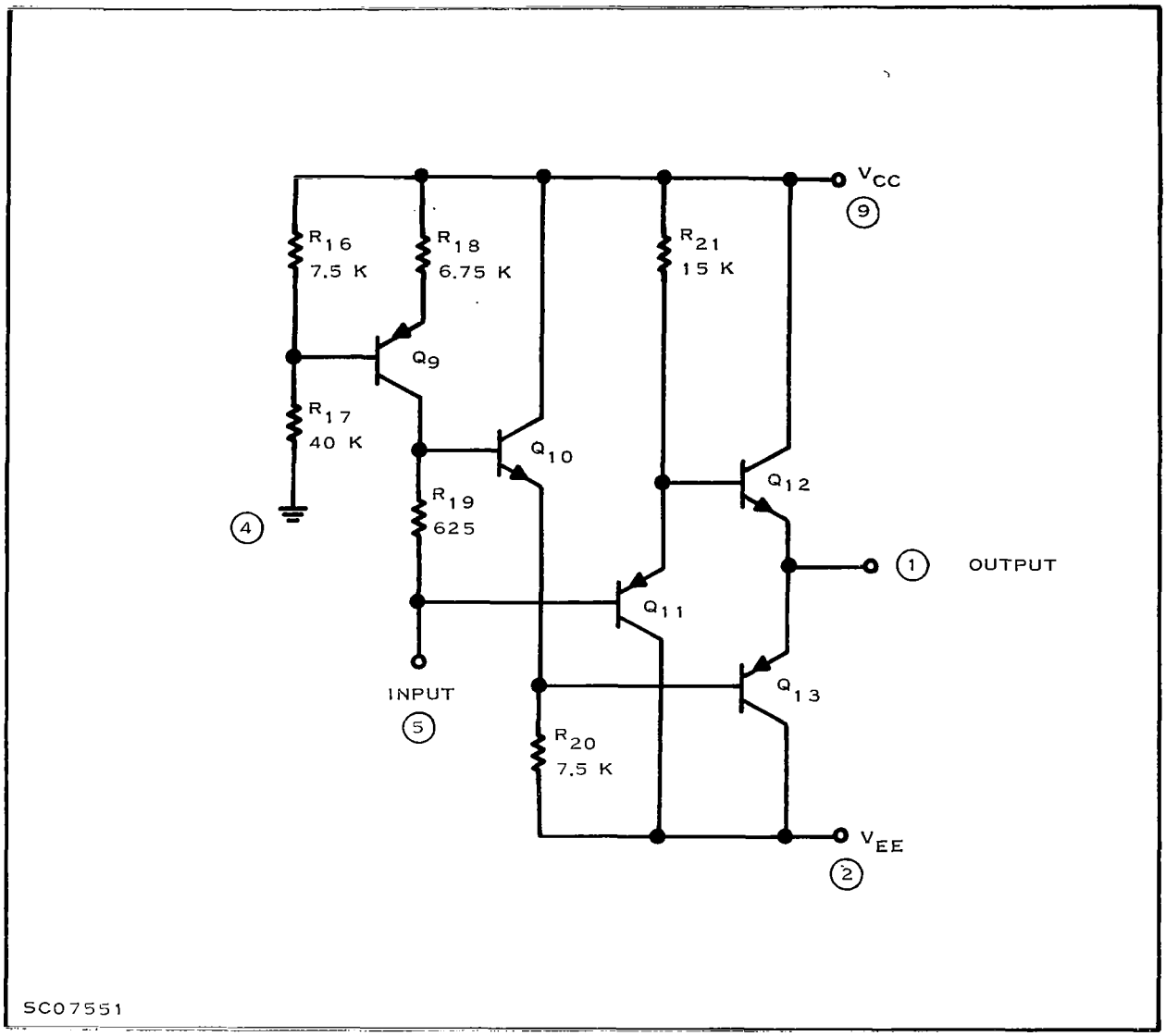


Figure 1-73. Class-B Power-Output Stage of SN526

The output impedance of the Class B stage is on the order of 20 Ω, and the output voltage swing, when biased from plus and minus 12 V, is 18 V_{p-p} into most loads.

It must be remembered that regardless of what the driving source for this Class B output stage is, it must provide a dc sink for the constant-current source current.

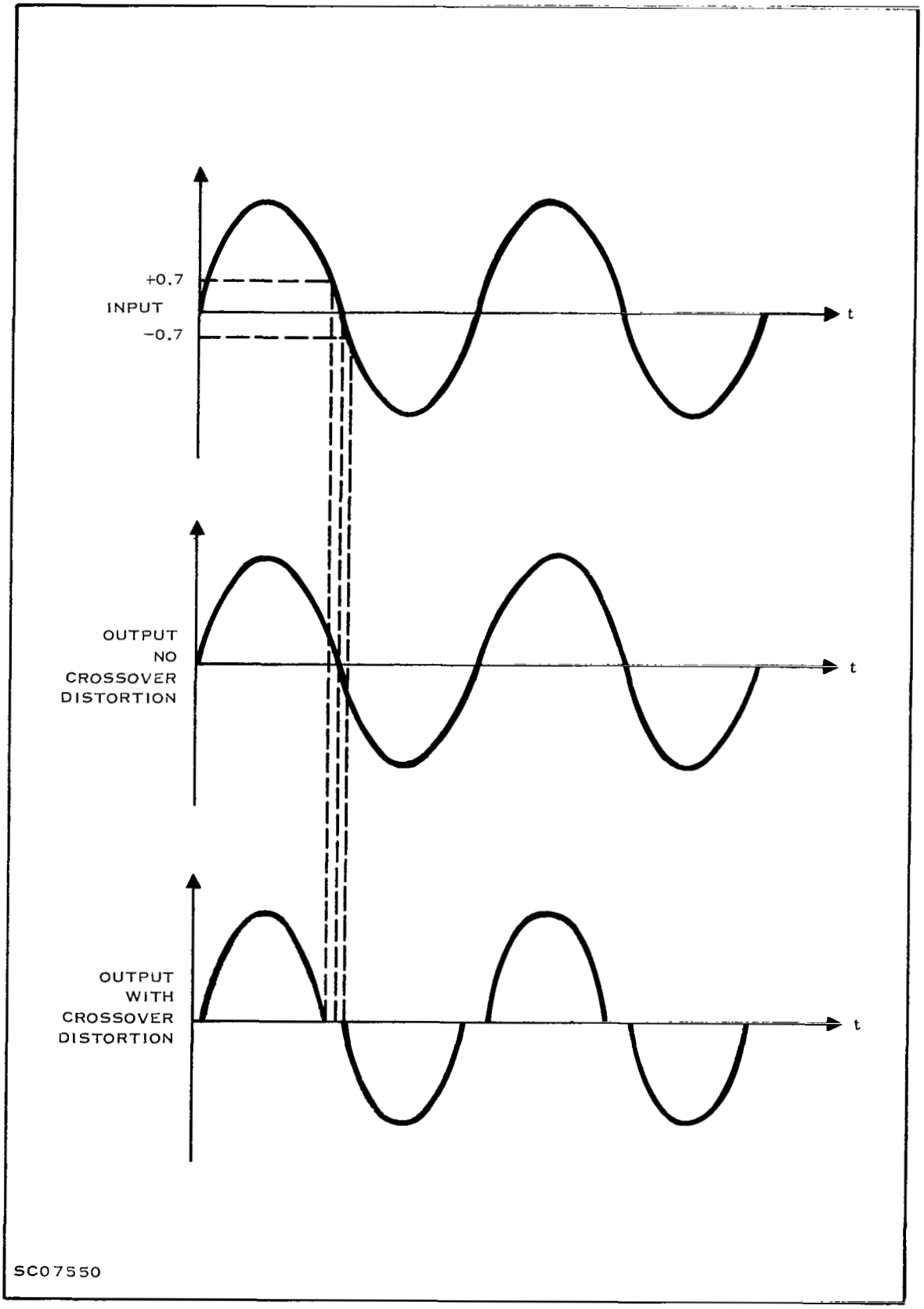
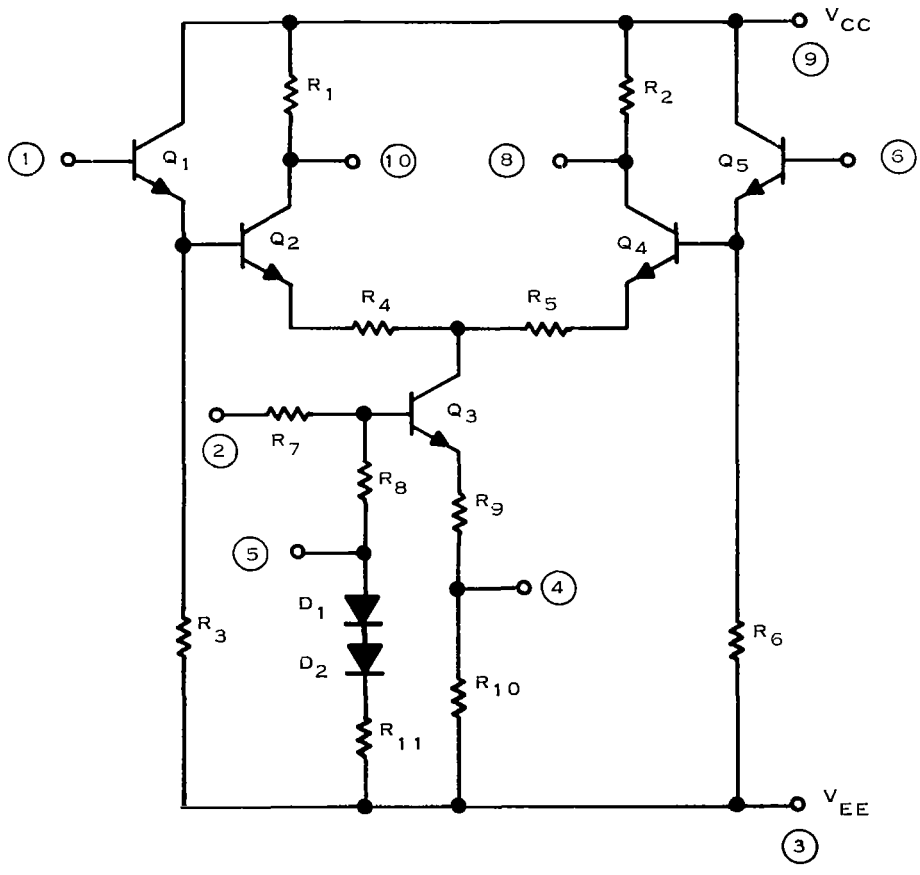


Figure 1-74. Crossover Distortion, SN526

3. Differential Amplifier (CA3000, RCA)

a. General

The CA3000 is a monolithic, silicon, differential dc amplifier, and it is shown in Figure 1-75. Primary features are an input impedance of 0.2 MΩ, common-mode rejection ratio of 98 dB, and AGC capability. Several modes of operation are possible by various connections of the network terminals.



SC07554

Figure 1-75. Differential Amplifier (CA3000, RCA)

b. Circuit Operation

Transistors Q_1 and Q_5 function as input emitter-followers to drive the differential-gain stage formed by Q_2 and Q_4. The primary function of the emitter-followers is to provide high input impedance. Transistor Q_3, when biased, acts as a constant-current source for the gain stage, which makes the output levels at pins 8 and 10 relatively insensitive to common-mode variations in signal- or dc level at the inputs. Resistors R_4 and R_5 provide emitter degeneration of the gain stage for increased bias stability and gain linearity. The output impedance is approximately equal to R_2 or R_3, or about 8 kΩ, and the maximum output voltage swing at pins 8 and 10 is 6.4 V_{p-p}, typically.

The input characteristics, such as input offset current and input offset voltage, are basically a function of the match in h_{fe} and V_{be} of the Q_1 and Q_2, and the Q_4 and Q_5 combinations.

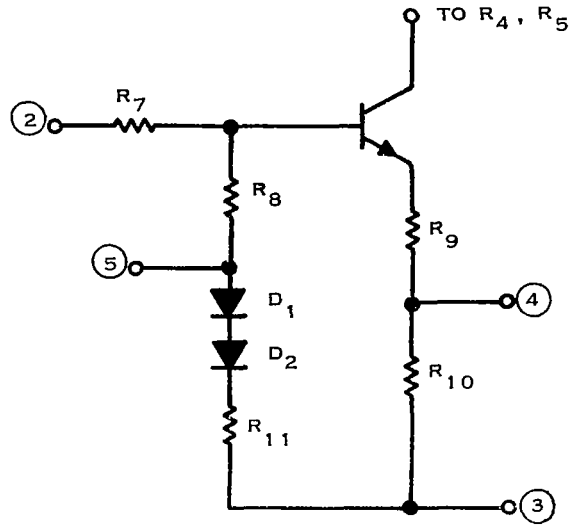
c. Modes of Operation

The current-source network is shown in Figure 1-76. The bias current in the second stage may be varied by adjusting the overall voltage between pins 2 and 3. Obviously, as the current is changed the output dc level, voltage gain, and output voltage swing are changed. In addition, since the emitter resistance, r_e, is temperature dependent and is contained in the gain and offset calculations, the temperature characteristics will be slightly different for each current-source bias. The four possible modes of operation are shown in Table 1-18.

Table 1-18. Possible Modes of Operation

Mode	Special Condition	Status of Diodes
1	No pins shorted	In
2	Pins 4 and 3 shorted	In
3	Pins 5, 4, and 3 shorted	Out
4	Pins 5 and 3 shorted	Out

These modes of operation are shown schematically in Figure 1-77 with pin 2 grounded. For each of the modes, with pin 2 grounded, the positive and negative supply voltages may be adjusted such that the output dc levels are at zero volts. Circuit performance factors are shown in Table 1-19 (RCA Note 5030) as funcations of the modes of operation for two negative supply levels, −3 V and −6 V.



SC07555

Figure 1-76. Gain-Stage Biasing Network of Ca3000

Table 1-19. Circuit Performance Factors (RCA Note 5030)

Mode	Supply Voltage (V_{cc})	(V_{ee})	Voltage Gain (dB)	Output Voltage (V_{dc})	Positive Voltage Swing	Negative Voltage Swing	P_t (mW)
1	6.0	6	31.2	+2.3	3.7	3.8	40.0
2	6.0	6	34.6	−1.5	7.5	0.0	61.0
3	6.0	6	32.4	+1.0	5.0	2.4	47.0
4	6.0	6	27.3	+4.3	1.7	5.7	36.0
1	3.7	6	31.2	0.0	3.7	1.4	33.0
2	10.6*	6	34.6	0.0	10.6	1.5	83.0
3	5.0	6	32.4	0.0	5.0	1.5	43.0
4	1.7	6	27.3	0.0	1.7	1.4	25.0
1	3.0	3	27.5	+1.2	1.8	2.6	8.8
2	3.0	3	32.6	−1.5	4.5	0.0	14.0
3	3.0	3	24.4	+1.9	1.1	3.3	8.5
4	3.0	3	16.6	+2.6	0.4	4.1	7.4
1	1.8	3	27.5	0.0	1.8	1.5	7.2
2	5.3	3	32.6	0.0	5.3	1.5	19.0
3	1.1	3	24.4	0.0	1.1	2.6	6.2
4	0.4	3	16.6	0.0	0.4	1.5	8.4

* Over rating.

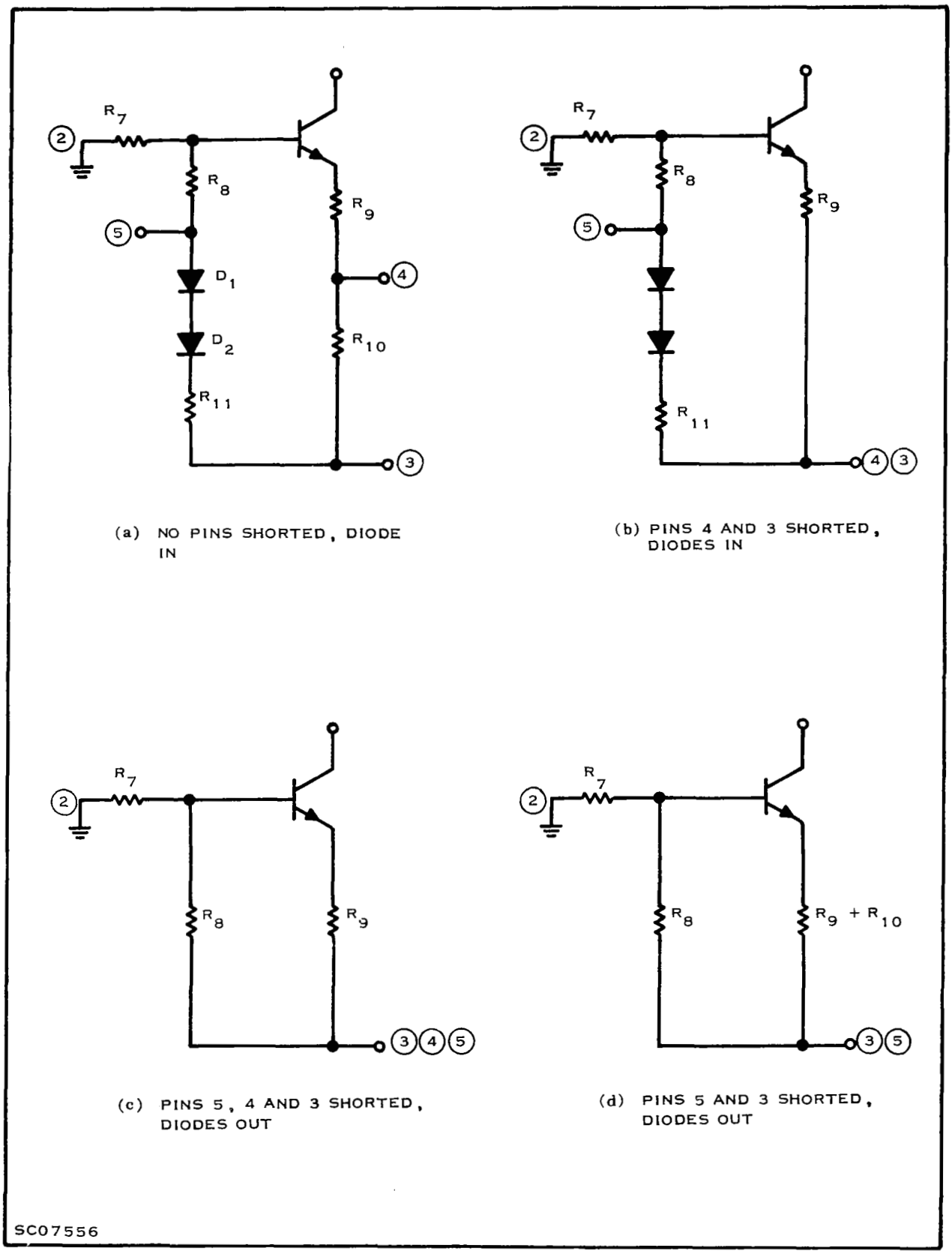
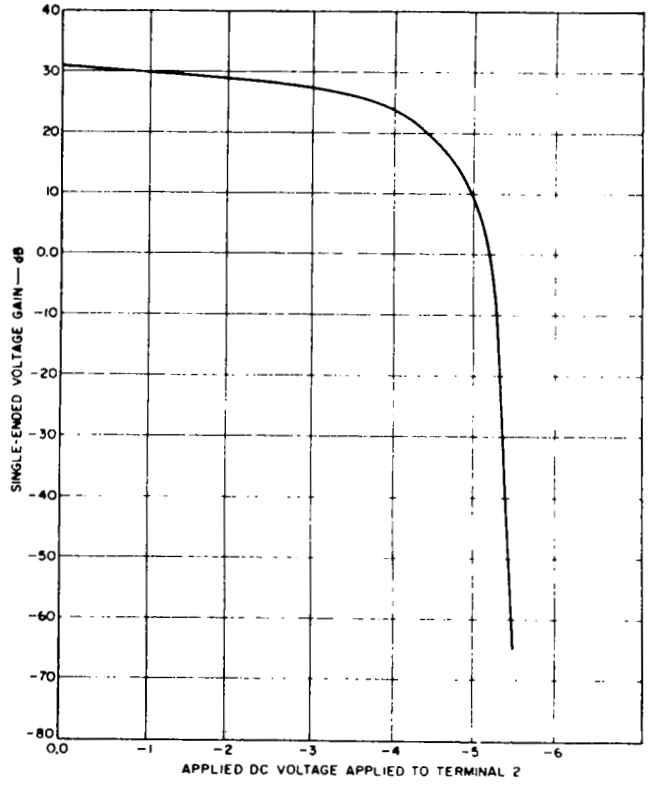


Figure 1-77. The Four Possible Modes of Operation for the CA3000

The amplifier may be AGC'd by using symmetrical supply voltages and varying the dc voltage on pin 2 from 0 to 5.5 V. The single-ended voltage gain can be varied over a 90-dB range, as shown in Figure 1-78. As the pin-2 voltage is decreased, the voltage across the current-source resistor drops, which causes less current to be drawn through gain-stage transistors Q_2 and Q_4. This causes their emitter resistance, r_e, to increase, since $r_e = KT/qI_e$. The differential voltage gain can be derived to be approximately $A \approx R_1/(r_e + R_4)$. Therefore, as r_e increases, the gain decreases. Notice that when r_e becomes large compared to R_4, the amplifier actually changes to a negative-gain operation. Detailed analysis of the entire circuit, which is beyond the scope of this discussion, would be required to show mathematically the reasons for the various temperature characteristics and bias levels.



SCO7475

Figure 1-78. Variation of Single-Ended Voltage Gain with Change of dc Voltage Applied to Terminal No. 2 (CA3000)

The amplifier is very versatile in that the pins available may be used to obtain an infinite combination of power dissipation, voltage swing, and gain. Manufacturer applications material should be considered for more detail on its usage.

4. Differential Comparator (μA711, Fairchild)

a. General

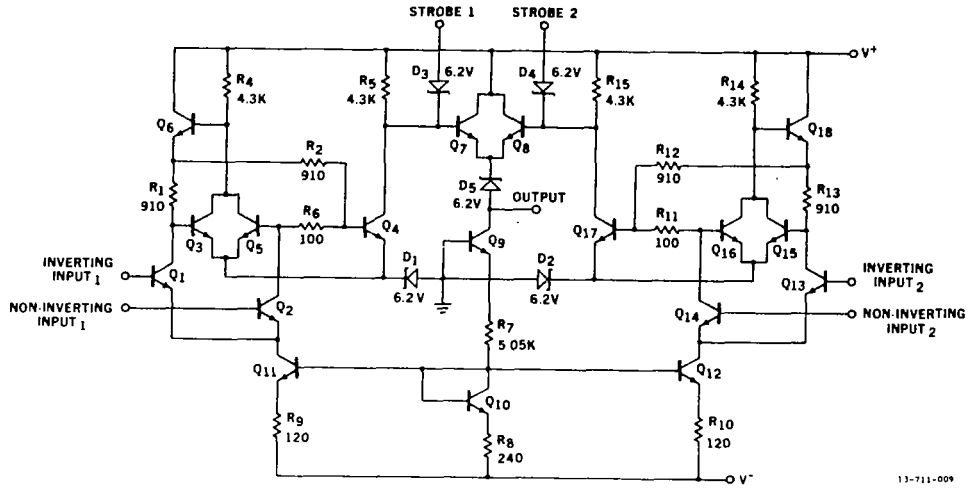
The μA711 has been selected to exemplify a typical differential comparator. The μA711 consists basically of two high-gain operational amplifiers on one silicon chip, with their single-ended outputs OR'd together. In general, its function is to compare two signal voltages and produce a digital "one" or "zero" at the output when one signal is more positive than the other. More specifically, whenever the noninverting input is more positive by several millivolts than the inverting input, the output rests at approximately +6 V.

Each of the two amplifiers, typically, has a gain of 1500, with an input voltage range of ±7 V. The differential input voltage is limited to ±5 V. Any greater difference between the two inputs can cause the base-emitter junction of the transistor accepting the most negative input to break down. This would couple the two signals together and could create erroneous outputs from the comparator. Additionally, if there were no current limiting on the input, damage could result to the circuit. Supplementing each comparator is a strobe or gating input which allows the designer to inhibit the output by clamping it to the logical "zero" state. If strobing is not required, the strobe points may be left unconnected. However, for maximum speed, it is suggested that the strobe be connected to the logic supply voltage (+6 V for this application).

The supply voltages required in most applications are +12 V and −6 V. With these voltages, the logic levels of the output are +6 V for a logical "1" and ground for a logical "0." A logical "one" output is present when the noninverting input is more positive than the inverting input. A logical "zero" is present when the inverting input is more positive. Obviously, the inputs could be reversed to invert the logic levels.

b. Circuit Description

The operation of the μA711 circuit can be explained by analyzing Figure 1-79, which shows the two comparators with their common output stage. This figure is the schematic as it appears on the μA711 data sheet published by Fairchild Seimconductor, which is included in a previous section of this volume of the Handbook. The description presented here specifically refers to the comparator on the left half of the schematic, but it applies to both comparators, since they are identical.



SCO7476

Figure 1-79. Schematic of Differential Comparator (μA711, Fairchild)

The inverting and noninverting inputs of the comparator feed the bases of a differential input stage, Q_1 and Q_2. The emitters of this input stage are attached to a current source, Q_{11}, which provides the common-mode rejection required by a comparator, by making the collector currents of Q_1 and Q_2 insensitive to the common-mode input voltage. The emitter of the constant-current source is biased about 250 mV above the negative supply to allow for the maximum swing of input voltages. The diode-connected transistor, Q_{10}, in the biasing circuit attached to Q_{11}, temperature-compensates for the base-emitter junction of Q_{11}; transistor Q_9 isolates the bias divider of Q_{11} from the output signal.

The collector resistors of the input stage, R_1 and R_2, are a pair of closely matched resistors, which are supplied from a constant-current source, Q_6. The matching of these resistors is very critical, because they provide the bias on the second stages, Q_3 and Q_4. Second-stage amplification is actually provided by Q_4, while Q_3, along with R_1, R_2, and R_4, provides a balanced biasing arrangement for the bases of Q_3 and Q_4. In parallel with Q_3 is Q_5; Q_5 is only operative when the inverting input is more positive than the noninverting input. The purpose of Q_5 is to reduce the base drive on Q_4 when Q_4 saturates, thus reducing both power dissipation and storage time. For either linear operation or with the noninverting input more positive than the inverting input, the collector current of Q_2 creates a sufficient voltage drop across R_6 to turn Q_5 "off." Collector resistor R_4 is common to Q_3 and Q_5 and defines the level of the voltage source, Q_6.

The zener diode, D_1, attached to the emitters of Q_3, Q_4 and Q_5, shifts their operating voltages to a higher level to allow for a large input-voltage range. An identical zener, D_5, shifts the output down to the normal logic levels.

The single-ended output at the collector of Q_4 drives the emitter-follower, Q_7. This output is OR'd together with the output of the second comparator, Q_3, and is shifted in voltage, by D_5.

Briefly, in review, if the noninverting input is more positive than the inverting input, Q_2 turns "on," Q_1 and Q_4 turn "off," and Q_7 turns "on," giving +6 V at the output. If the inverting input is more positive than the noninverting input, Q_1 turns "on," Q_2 and Q_3 turn "off," Q_4 remains "on" with Q_7 "off," and the output rests at ground.

c. Typical Application: Window Discriminator

(1). General. The simplified schematic shown in Figure 1-80 depicts a window discriminator that is used for selecting pulses of either polarity below or above a specific amplitude. The plus inputs represent the noninverting inputs, and the minus inputs represent the inverting inputs. The theory of operation will be presented next.

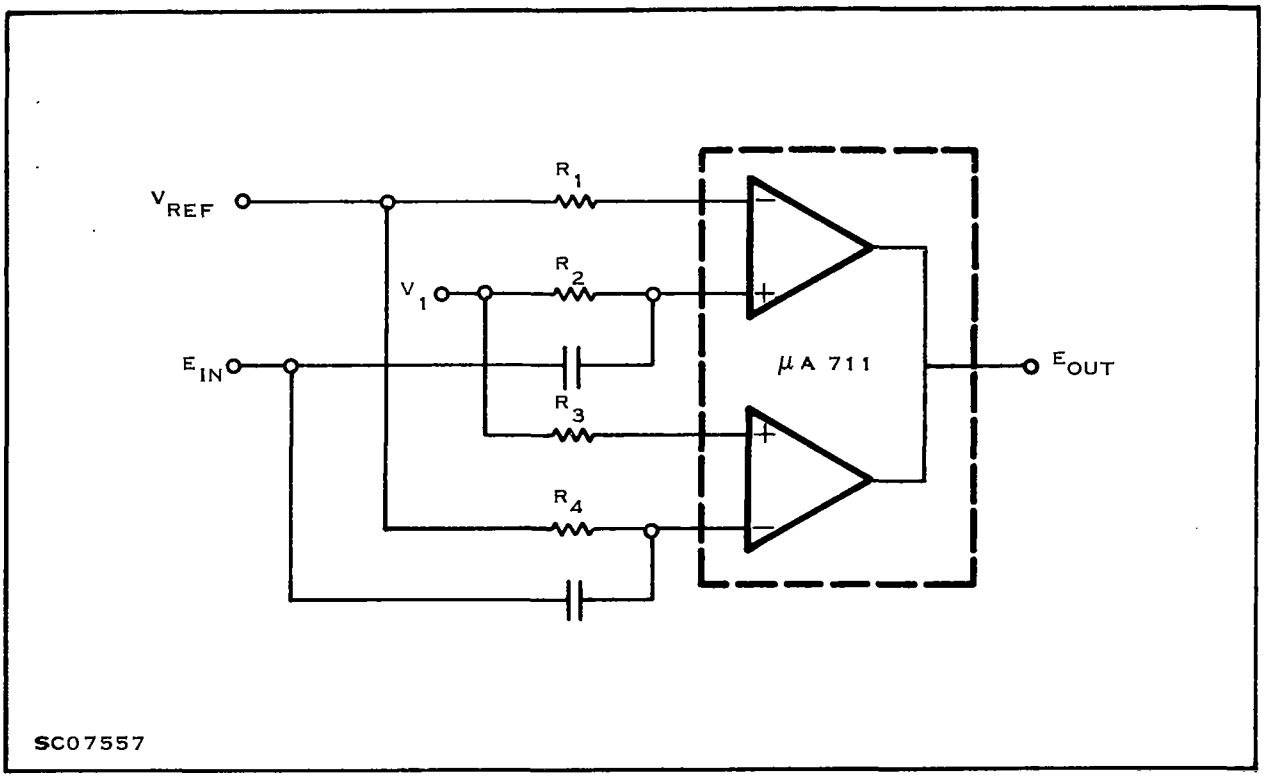


Figure 1-80. Window Discriminator (Simplified Schematic, μA711)

(2). Theory of Operation. Whenever a positive pulse of amplitude greater than $|V_{ref} - V_1|$ is applied, an output pulse will occur at E_{out} of approximately the same duration as the input pulse. This is true, since the pulse is coupled to the plus input attached to R_2; whenever this point is more positive than the minus input of the same comparator, a positive output is present. For positive input pulses with amplitude less than $|V_{ref} - V_1|$, no output will occur.

Whenever a negative input pulse of amplitude greater than $|V_{ref} - V_1|$ is applied, an output pulse will occur at E_{out} of approximately the same duration as the input pulse. This is true because the pulse is coupled to the minus input attached to R_4. Whenever this point is more negative than the plus input of the same comparator, a positive output is present. For negative pulses with amplitude less than $|V_{ref} - V_1|$, no output will occur.

For best results, R_1, R_2, R_3, and R_4 should all be equal and as small as is practical, to minimize the error created by different input currents in the two comparators. But the resistors cannot be made too small, since the impedance seen by the input pulse is the parallel combination of R_2 and R_4. The effect of the preceding error is to center the window about some point offset from V_1. It is also very important that the maximum differential input voltage not exceed the 5 V specified on the data sheet.

Power supply variations are not too critical, but they do affect circuit performance. For instance, variations in the positive supply affect the circuit in two ways. First, the positive supply directly controls the amplitude of the output pulse, which is roughly B^+ minus 7 V. And second, variations in the positive supply vary the upper level of the input voltage range. Variations in the negative supply affect the lower level of the input voltage range.

5. Conclusions

The three linear microcircuits which have been discussed are representative of a large percentage of those presently in existence. Although there are amplifiers, both differential and operational, with bandwidths ranging from a few kHz to 50 MHz, and gains ranging from 20 dB to 100 dB, the basic circuit configurations are similar to those that have been discussed here. The differences in amplifier performance and frequency response are due primarily to construction and process variations and not, in general, to circuit configurations. This primary cause, construction-process variation, is independent of the design application, whether it be AF, IF, RF, dc or video.

D. SYSTEM DESIGN USING LINEAR MICROCIRCUITS

1. Manufacturer Data Sheets

One of the most important aspects of performing system design with microcircuits is the correct interpretation of manufacturers' data sheets. A few typical linear microcircuit data sheets are included in the Appendix. The terms defined earlier will aid considerably in this interpretation. There are, however, some additional points which are sometimes confusing.

One of the most often misinterpreted parameters is the maximum peak-to-peak output voltage (V_{om}). If the amplifier is single ended, there is no confusion. However, many differential amplifiers are specified in a manner that is somewhat confusing unless the user is familiar with the terminology. This parameter is often specified differentially and can best be interpreted with the use of a figure. The diagram shown in Figure 1-81 illustrates the differential outputs for a sinusoidal input. The peak-to-peak voltage is defined by the following equations and is the voltage that would be read on a peak-reading VTVM connected between the differential outputs:

$$V_{(diff)1} = V_{P(out)1} - V_{P(out)2} = V_P - (-V_P) = 2V_P \tag{7}$$

$$V_{(diff)2} = V_{P(out)1} - V_{P(out)2} = -V_P - V_P = -2V_P \tag{8}$$

$$V_{om} = V_{(diff)1} - V_{(diff)2} = 4V_P \tag{9}$$

where

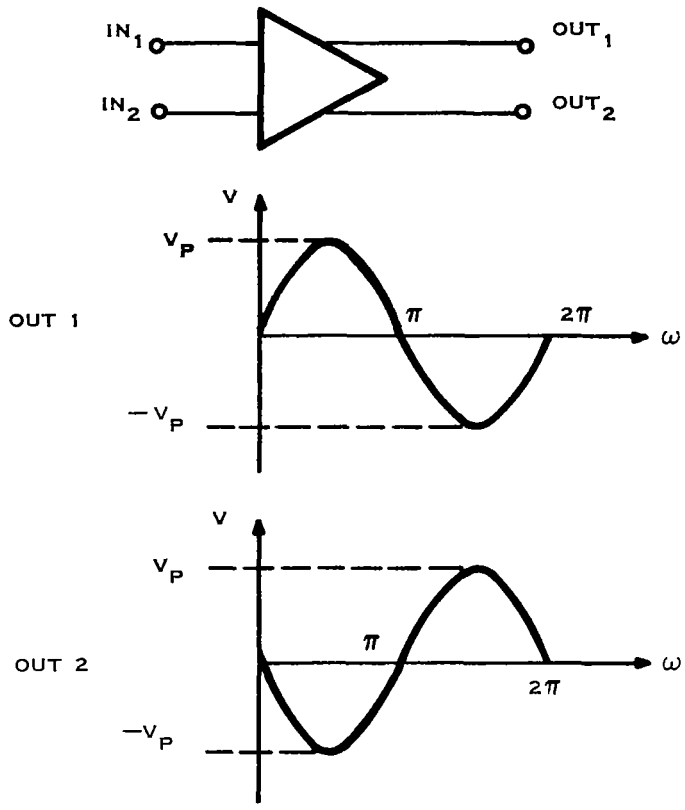
V_P = maximum single-ended peak voltage.

As an example, consider the Texas Instruments SN523A data sheet, shown in the Appendix. The maximum peak-to-peak voltage is specified as 24 V, typically. This can be interpreted as:

$$V = \frac{V_{om}}{4} = \frac{24}{4} = 6 \text{ V}$$

Thus, the maximum peak single-ended voltage is 6 V.

The majority of the remaining parameters are straight-forward when considered in light of the definitions given previously herein. However, there is one remaining parameter which merits discussion—the specified power dissipation. Before discussing derating as it applies to reliability, it is necessary to explain the related parameters and the design techniques that have been found to be most useful for obtaining the maximum allowable power dissipation.



SC07558

Figure 1-81. Interpretation of V_{om}

There are four major parameters that the circuit design engineer must consider to obtain the maximum allowable power dissipation:

- Package selection.
- Temperature range.
- Bar mount.
- Circuit power dissipation.

These parameters are all related by two factors: the maximum allowable junction temperature in the microcircuit, and the thermal resistance of the particular package

being considered. Since the temperature range over which the circuit is to operate is predetermined, these parameters are used to determine the maximum allowable power dissipation for reliable operation. Perhaps the best way to illustrate this procedure is with the use of an example.

Assume that the thermal resistance, ${}_{j}\theta_{A}$, of a particular package, with the microcircuit alloyed to the package, is 0.3 °C/mW. Further, assume that the maximum allowable junction temperature for the process being utilized is 175°C. If the temperature range over which the device is to be operated is from −55°C to + 125°C, the maximum allowable power dissipation can be computed as follows:

$$\theta_{jA} = \frac{T_j - T_a}{P_{max}} \tag{10}$$

$$P_{max} = \frac{T_j - T_a}{\theta_{jA}}$$

where

θ_{jA} = thermal resistance, °C/mW between junction and ambient.

T_j = junction temperature, °C

T_a = ambient temperature, °C

P_{max} = maximum power dissipation

For this example:

$$P_{max} = \frac{175° - 125°}{0.3} = 167 \text{ mW}$$

The preceding information has been introduced here primarily to point out that a microcircuit has been "derated" by the very nature of the design technique used by the design engineer. It is possible to further increase the reliability by reducing the power supply voltage, and thus the power dissipation. However, this generally results in a loss of performance, and at any rate, it is not necessary, due to allowances made previously by the design engineer.

2. Application and Design Rules

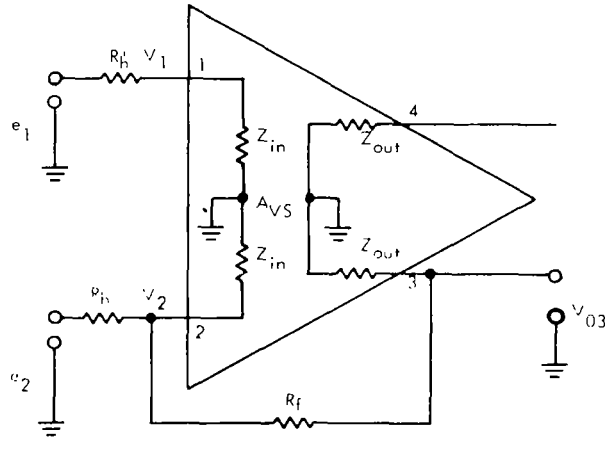
a. General

Since the largest percentage of linear microcircuits presently available have the basic differential amplifier configuration, this type of circuit will be discussed here in detail.

The high-gain differential amplifier can be utilized differentially or if operated single ended, as an operational amplifier. The two major factors to be considered in the operation of this type of amplifier are conventional feedback theory and amplifier frequency compensation.

b. Closed-loop Amplifiers and Feedback Theory

(1). General. The circuit in Figure 1-82 represents a basic configuration for a closed-loop differential amplifier. The following are definitions of terms and parameters that will be used in deriving the equations for closed-loop amplifiers:



SCO7478

Figure 1-82 Closed-Loop Differential Amplifier

- A_{vs} (Single-ended voltage gain). The ratio of change in the single-ended output voltage (V_{03}) to a change in the differential input voltage (V_1-V_2). The equation for A_{vs} is:

$$A_{vs} = \frac{V_{03}}{V_1 - V_2} \tag{11}$$

- A_{vd} is the differential voltage gain and is equal to 2 A_{vs}.
- Z_{in} (Input impedance). The impedance between either input terminal and ground with the other input terminal grounded and the outputs balanced (open-circuit amplifier).
- Z_{out} (Output impedance). The impedance between any output terminal and ground when the outputs are balanced (open-circuit amplifier). The feedback network is composed of R_f and R_h, and for a particular application they may be complex values.
- A_{CL} (Closed-loop voltage gain). The ratio of change in the output voltage to a change in the input source voltage with feedback applied. The equation for A_{CL} is:

$$A_{CL} = \frac{V_O}{E_{in}} = \frac{KG}{1 + KGH} \tag{12}$$

where

K = dc voltage gain

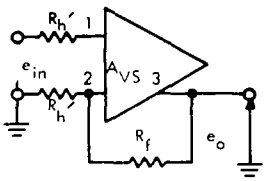
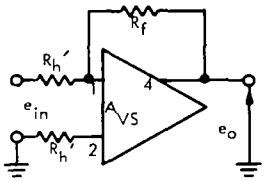
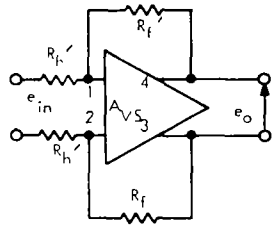
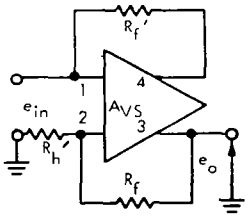
G = frequency-variant term

H = output voltage that is fed back to the input terminal

Equation (12) represents the voltage gain for any closed-loop configuration and will be used in this discussion to analyze feedback-amplifier configurations.

(2). Noninverting Amplifiers. The circuit of Figure 1-77 and its variations form the bulk of commonly used differential amplifier configurations; normally, one of the source-voltage terminals (e_1 or e_2) is connected to ground. By grounding terminal e_2, the circuit of Figure 1-77 becomes a simple noninverting amplifier, as shown in circuit A of Figure 1-83. For this configuration, R_h is normally the source impedance of the signal voltage, e_1, KG is nearly equal to the open-loop transfer function A_{vs}, and the feedback ratio H is nearly equal to $R_h/(R_f + R_h)$. The exact values of KG and H can be obtained by taking into account the input and output impedances

Table II. Interface Parameters

Closed-Loop Configuration	Closed-Loop Voltage Gain $A_{CL} = \frac{KG}{1+KGH}$ KG	H	Transfer Impedance $Z_T = \frac{V_o}{i_{in}}$	Closed-Loop Impedances Input(Z'_{in})	Output(Z'_o)	Comments
A. 	A_{VS}	$\frac{R_h}{R_h+R_f}$		High Unstable $Z_{in}(1+KGH)$	Low Unstable $\frac{Z_{out}}{1+KGH}$	Noninverting Amplifier. If $KG \gg \frac{1}{H}$, Then $A_{CL} \approx \frac{R_f+R_h}{R_h}$
B. 	$-A_{VS}\frac{R_f}{R_h+R_f}$	$-\frac{R_h}{R_f}$	$\frac{A_{VS}R_f}{1+A_{VS}} \approx R_f$	Low $R_h + \frac{R_f}{1+A_{VS}} \approx R_h$	Low Unstable $\frac{Z_{out}}{1+KGH}$	Inverting Amplifier. If $KG \gg \frac{1}{H}$, Then $A_{CL} \approx -\frac{R_f}{R_h}$ Terminal 1 Ideal Summing Point.
C. 	$-2A_{VS}\frac{R_f}{R_h+R_f}$ $R = R'$	$-\frac{R_h}{R_f}$	$\approx R_f$	Low $2\left(R_h + \frac{R_f}{1+A_{VS}}\right) \approx 2R_h$	Low Unstable $\frac{2Z_{out}}{1+KGH}$	Differential Input — Output Amplifier.
D. 	A_{VS}	$\frac{R_h}{R_h+R_f}$	$\frac{A_{CL}R_f'}{1+A_{CL}}$	Stable $\frac{R_f'}{1+A_{CL}}$	Low Unstable $\frac{Z_{out}}{1+KGH}$	Modified Noninverting Amplifier. Good for Low-Noise, Stable-Input-Impedance Amplifier.

SC07949

Figure 1-83. Interface Parameters

of the amplifier. Using Equation (12), the closed-loop voltage gain is given in Equation (13):

$$A_{CL} = \frac{KG}{1 + KGH} = \frac{A_{vs}}{1 + A_{vs} \cdot \frac{R_h}{R_h + R_f}} \tag{13}$$

The same expression could be obtained from Equation (11) by setting e_2 equal to zero and solving for V_1 and V_2 in terms of e_1 and V_{03}.

When the other source voltage, e_1, is grounded, the amplifier in Figure 1-82 becomes a simple inverting amplifier (Circuit B, Figure 1-83). The expression for the closed-loop voltage gain is:

$$A_{CL} = \frac{V_{03}}{e_2} = \frac{-A_{vs} \cdot \frac{R_f}{R_h + R_f}}{1 + A_{vs} \cdot \frac{R_f}{R_h + R_f} \cdot \frac{R_h}{R_f}} \tag{14}$$

For the inverting amplifier, R_h is used for balancing the impedance connected to the input terminals and should be equal to $R_h R_f/(R_h + R_f)$.

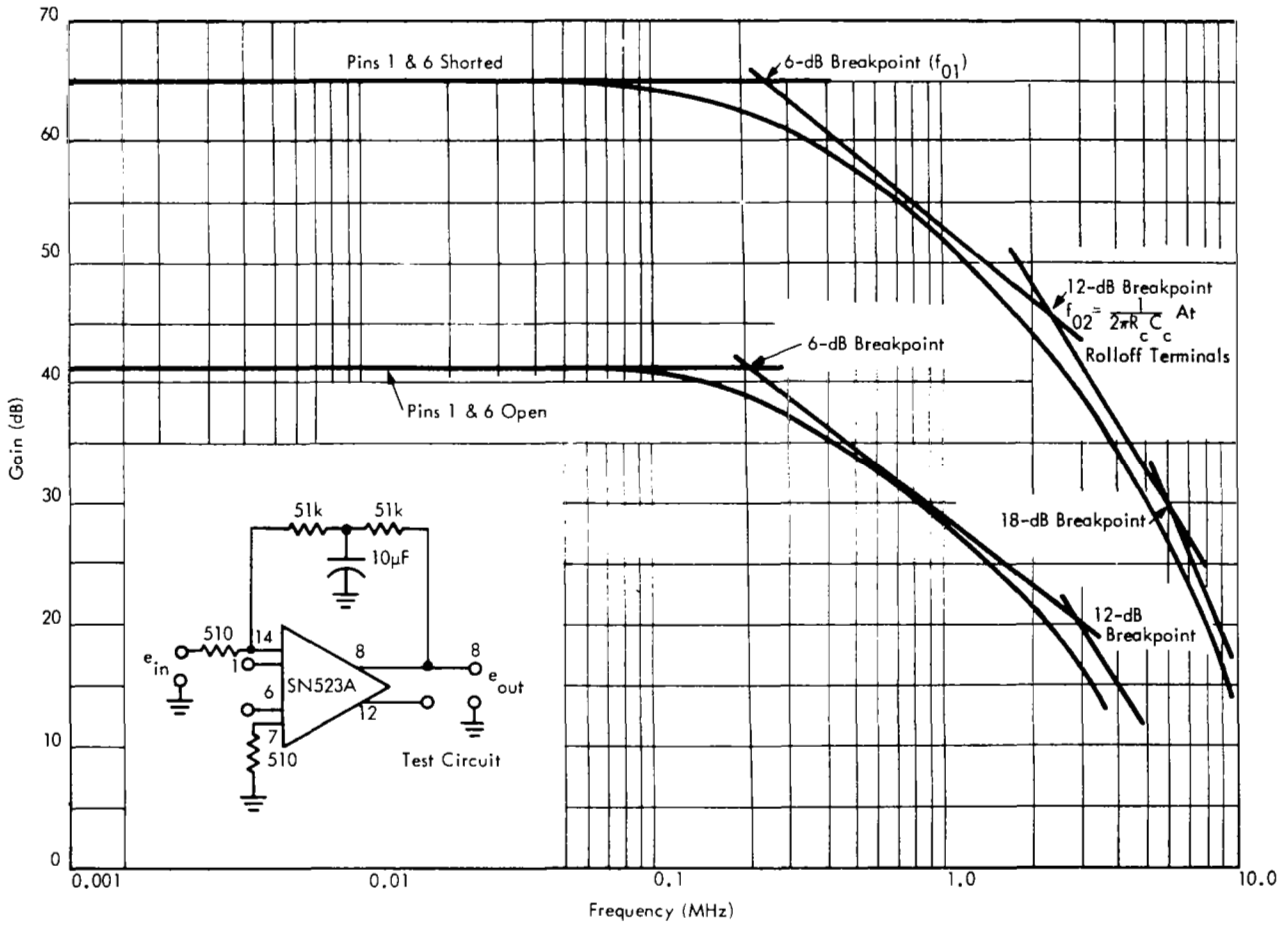
The two basic circuits discussed here, plus two modified circuits and their interface parameters, are listed in Figure 1-83. These are not the only applications of differential amplifiers, because the basic circuits can be used as a summing amplifier, an integrator, a differentiator, and for many additional applications.

c. Frequency Response and Compensation

(1). Frequency Response of Amplifiers. It is well recognized that negative feedback improves the performance of an amplifier. However, to design a stable system (one which will not oscillate), careful consideration must be given to the amplifier open-loop characteristics.

One of the most effective methods for quickly surveying an amplifier's frequency response is with the use of a Bode gain-versus-frequency plot. Shown in Figure 1-84 is a typical open-loop frequency response curve for a differential amplifier. A Bode plot shows that the voltage gain is a complex equation and can be expressed in a form similar to the following:

$$A_{vs} = \frac{A}{\left(\frac{S}{\omega_1} + 1\right)\left(\frac{S}{\omega_2} + 1\right)\left(\frac{S}{\omega_3} + 1\right)} \tag{15}$$



SCO7477

Figure 1-84. Frequency Response

where

A = at dc

ω_1 = the first break frequency, $(f_{01} \cdot 2\pi)$

ω_2 = the second break frequency, $(f_{02} \cdot 2\pi)$

ω_3 = the third break frequency, etc. $(f_{03} \cdot 2\pi)$

This complex voltage gain equation (Equation (15)) contains another useful parameter which can be obtained from the Bode plot—the amplifier phase-shift-versus-frequency plot. There is a direct correlation between amplifier rolloff rate (rate at which the amplifier gain decreases with frequency) and the amplifier phase shift. This relationship is shown in Figure 1-85 and is given in Equation (16):

$$\Phi = \frac{-n\pi}{2} \tag{16}$$

where

Φ = the phase shift in degrees

n = proportional to the slope of the gain curve or the rolloff rate in dB/octave divided by six.

When negative feedback is applied to an amplifier, certain conditions must be considered in order to prevent oscillations. These conditions can best be illustrated using the closed-loop gain equation:

$$A_{CL} = \frac{KG}{1 + KGH} \tag{13}$$

where

KG = Equation (14)

H = feedback factor

The term (1 + KGH) is a direct measurement of the improvement in the amplifier characteristics. However, this term must be greater than zero for all frequencies or the system will be unstable. Oscillations occur when KGH is equal to unity and the phase shift is equal to 180 degrees. Therefore, to prevent oscillations, KGH must be less than unity at the frequency where KGH has a phase shift of 180 degrees. It is apparent from Equation (15) and the open-loop Bode plot that there is a frequency at which the amplifier phase shift equals 180 degrees, i.e., the slope of the curve is 12 dB/octave.

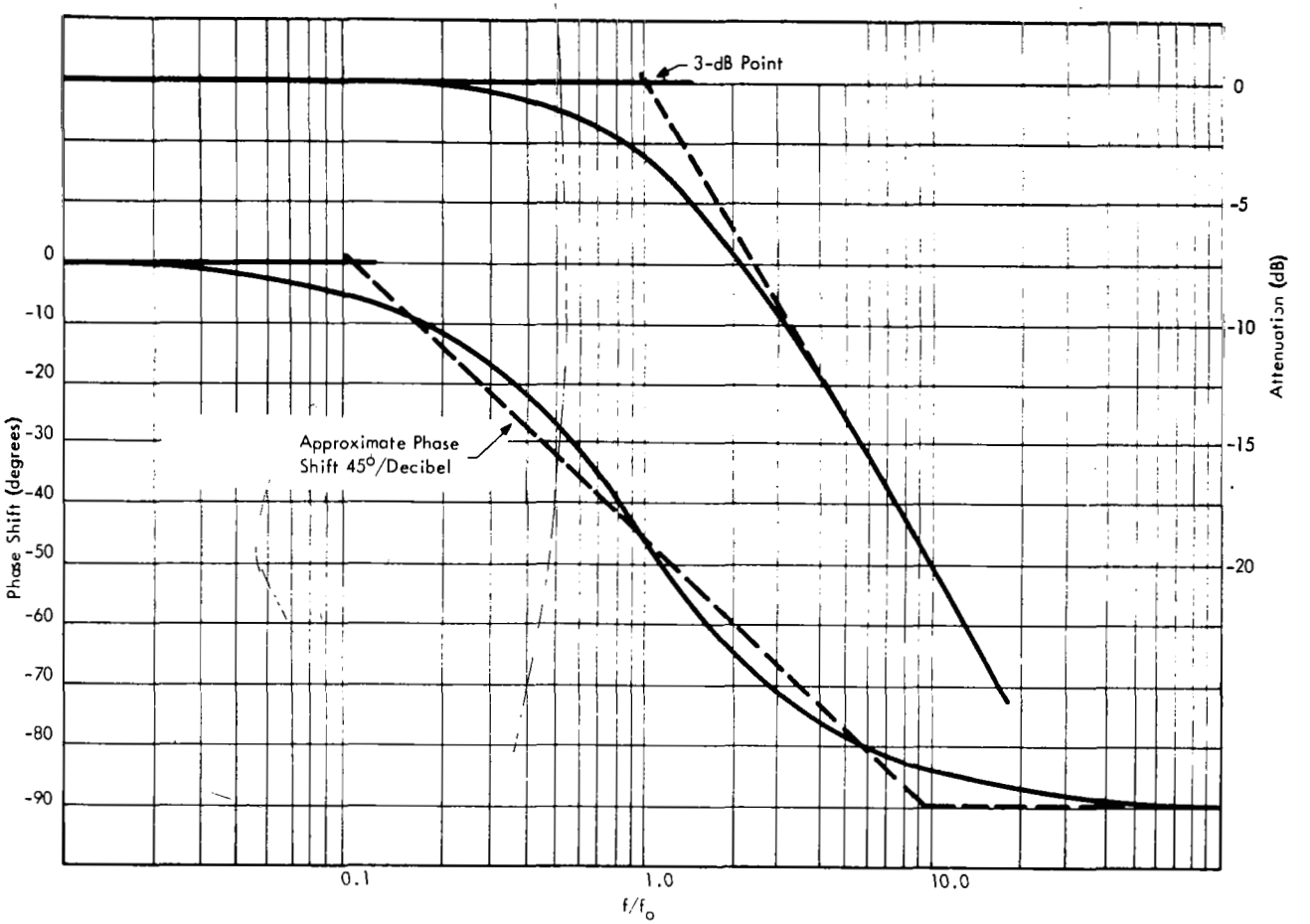


Figure I-85. Attenuation and Phase Shift for $1/(1 + jf/f_0)$

A typical Bode plot of differential amplifier open-loop voltage gain and phase shift is shown in Figure 1-86. At 4.2 MHz there is a phase shift of 180 degrees, and if 31 dB or more of feedback is applied, the amplifier will oscillate. It is, therefore, necessary to frequency-compensate the amplifier in applications requiring large amounts of feedback. This compensation must be of a form such that the amplifier rolloff rate does not exceed 12 dB/octave until KGH is less than unity. In addition, it is necessary to allow a safety margin to provide for differences in production units.

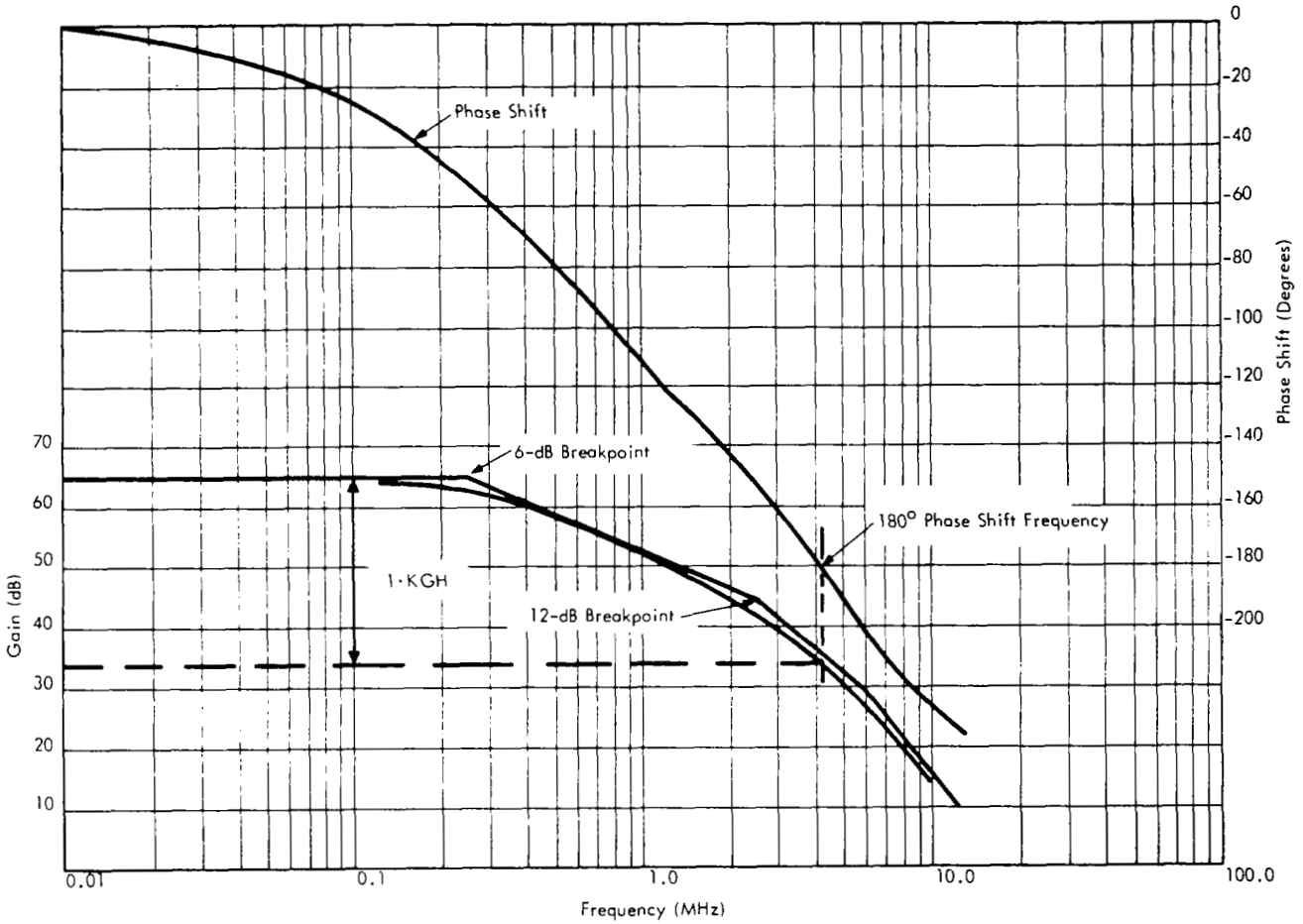
One safety factor that is obtained from the Bode plot is phase margin (Φ_m), defined as 180 degrees minus the phase angle that occurs when KGH equals one. For example, if the phase shift were limited to 90 degrees (rolloff rate of 6 dB/octave) until KGH < 1, this would correspond to a phase margin of 90 degrees. When the phase margin is less than 90 degrees, the closed-loop response will be peaked at the frequency where KGH equals unity. The amount of peaking is a function of phase margin as shown in Figure 1-87. It is recommended that at least 45 degrees of phase margin (9 dB/octave slope) be allowed so as not to have more than 3 dB of peaking.

(2). Frequency Compensation Techniques. It can be seen from the open-loop Bode plot, Figure 1-86, that there is a limited amount of negative feedback that can be applied to the amplifier and still have a stable system. To prevent a 12 dB/octave slope before KGH equals unity, for large values of H the open-loop gain at high frequencies must be decreased by frequency compensation.

The simplest method of frequency-compensating an amplifier is to connect a large capacitor between some signal point and ground such that it causes the frequency response to roll off at a rate of 6 dB/octave at a relatively low frequency (Curve 1 of Figure 1-88). This is a satisfactory method for frequency-compensating an amplifier for dc or very-low-frequency applications, and any amount of feedback can be applied without causing oscillations. However, this severely limits the bandwidth, and for wide-bandwidth applications the natural rolloff of the amplifier should be used to provide some of the required frequency compensation. From Curve 2 in Figure 1-88, it can be seen that by this method the bandwidth has been increased considerably.

Before continuing with frequency compensating techniques, it is necessary to define several terms that will be used and to analyze the cause and effect of breakpoints. First, the equation for frequency f, is as follows:

$$f_1 = \frac{1}{2\pi R_c C_1} \qquad (17)$$



SCO7481

Figure 1-86. Open-Loop Voltage and Phase Shift

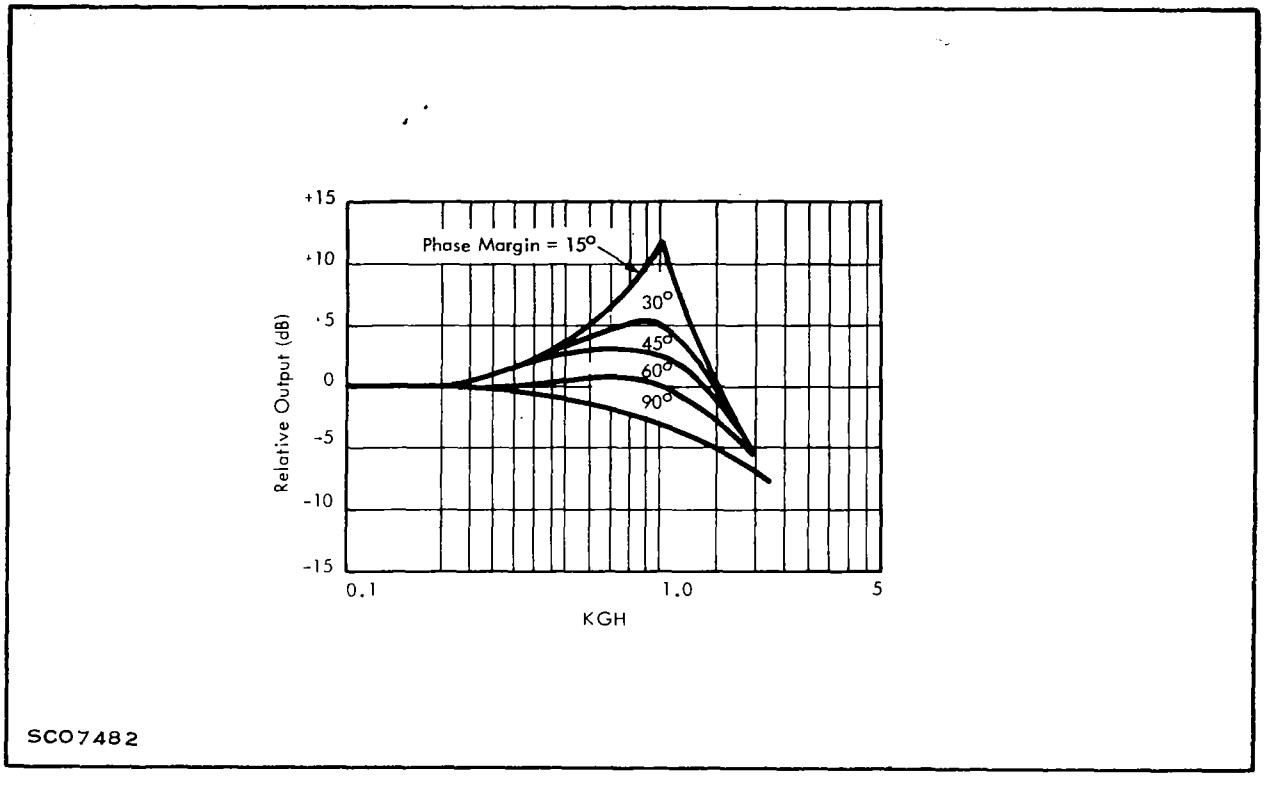


Figure 1-87. Peaking as a Function of Phase Margin

where

R_c = amplifier internal resistance at the rolloff terminal.

C_1 = external capacitor which is connected to the rolloff terminal to provide a pole (breakdown) at the frequency f_1 corresponding to the R_cC_1 time constant.

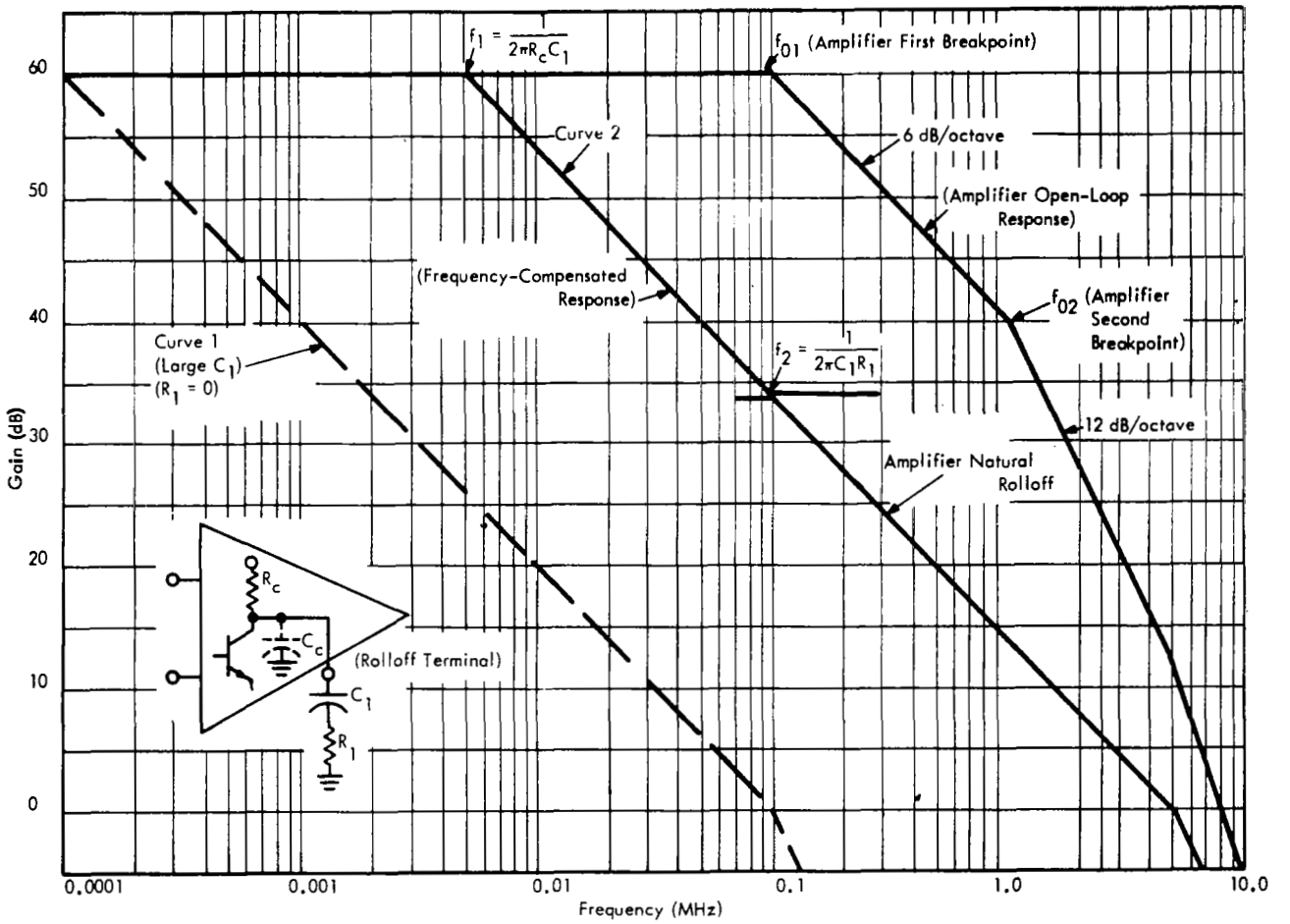
The equation for frequency f_2 is:

$$f_2 = \frac{1}{2\pi C_1 R_1} \tag{18}$$

where

R_1 = external resistor connected in series with C_1 to provide a zero (break up) at the frequency f_2 corresponding to the C_1R_1 time constant.

In Figure 1-88 are shown the breakpoints at f_1 and f_2 that are due to the compensating network, R_1 and C_1.



SCO7480

Figure 1-88. Amplifier Rolloff

The majority of microcircuit amplifiers have special terminals for frequency compensation. They consist of points connected to the collectors of an amplifying stage in such a manner that the collector load, R_c, can be shunted by an external impedance.

It can be seen in Figure 1-88 that the second breakpoint (at f_{02}) did not occur at 1.0 MHz for the compensated response as it did in the open-loop response. This illustrates an important point in frequency-compensating an amplifier for wide-bandwidth applications—it is necessary to determine what causes the open-loop response breakpoints. In Figure 1-88, the second breakpoint was assumed to be caused by internal capacitance, C_c, shunting the collector load, R_c. When C_1 is added, a new breakpoint appears at f_1 and the original breakpoint is moved to a higher frequency that is determined by C_c and R_1 in parallel with R_c. If the first breakpoint of the open loop was caused by the R_cC_c time constant, the f_2 break-up point would be added at the second f_{02} breakpoint instead of the first breakpoint f_{01}.

One additional technique to use in frequency compensation is to place a capacitor, C_f, across the feedback resistor, R_f. This, in effect, decreases the closure rate at which the open-loop and closed-loop curves converge, and it reduces the phase angle of KGH during the open-loop 12 dB/octave region. The addition of C_f decreases the closed-loop response peaking and improves the stability of the system. The value of C_f is calculated using the following equation:

$$C_f = \frac{1}{2\pi R_f f_x} \tag{19}$$

where

R_f = value of feedback resistor

f_x = frequency at which the closed loop response crosses the compensated open-loop response (the frequency where KGH equals unity)

To be presented here is a general procedure for frequency compensation in designing wide-bandwidth closed-loop amplifiers. To maintain a slope less than 12 dB/octave before KGH equals unity, a 6-dB/octave line is drawn from the point of intersection of the closed-loop gain line and the open-loop response. The point of intersection of the open-loop gain and the 6-dB/octave line is the required first-break frequency, f_1. Therefore, rearranging Equation (17):

$$C_1 = \frac{1}{2\pi R_c f_1} \tag{17}$$

If the addition of C_1 shifted f_{01} to f_1, the value of R_1 is:

$$R_1 = \frac{1}{2\pi C_1 f_{01}} \tag{18}$$

If the addition of C_1 shifted f_{02} to f_1, then the value of R_1 is:

To take into account the variation in characteristics with ambient conditions, f_1 should be chosen an octave lower than is indicated by the preceding procedure. However, the point where the effect of C_1 is removed by R_1 (i.e., the zero due to R_1C_1) should not be lowered from the f_{01} or f_{02} points.

If a third open-loop breakpoint is present near to the intersection of A_{OL} and A_{CL}, a capacitor, C_f, is added across the feedback resistor to reduce the phase shift of KGH. From Equation (19):

$$C_f = \frac{1}{2\pi R_f f_x} \tag{19}$$

where

f_x = the frequency where A_{OL} and A_{CL} intersect.

Note that some shifting can occur in both f_{01} and f_{02} by the addition of C_1. Therefore, to obtain an accurate value of R_1, it is often necessary to plot the open-loop response with frequency compensation added and empirically determine the value of R_1. This is also necessary when using large source impedances.

When two rolloff terminals are available on the same amplifying stage, the compensation network (R and C) should be connected between the two terminals instead of between one terminal and ground. Therefore, the value of R_c will be doubled. This will reduce the necessary capacitance of C_1 by a factor of two and will double the necessary resistance of R_1, thus reducing the loading effect.

3. Additional Considerations

There are numerous additional factors to be considered when using linear microcircuits in system design. These considerations will be discussed with reference to the design procedure for incorporating a microcircuit amplifier in a hypothetical system design where a closed-loop stable amplifier is required. The design procedure, including the primary considerations for correct circuit application and maximum system performance, is as follows:

- After selecting an amplifier to meet the requirements for bandwidth, gain, input and output impedance, power supply, etc., determine the open-loop frequency response by referring to the manufacturer's application notes or to empirical data.
- Determine the feedback configuration and the necessary frequency compensation for the particular application, as previously described herein. The following is a list of design alternatives which will improve system performance:
    - Provide a dc ground return for both amplifier inputs, and whenever possible keep the source impedance small relative to the input impedance of the amplifier.
    - Provide dc offset to compensate for the internal-amplifier offset. This can be achieved with a resistor divider network at the input and is necessary in cases where the system has high gain and/or is dc coupled.
    - Allow for maximum phase margin, depending on required bandwidth.
    - Design the frequency-compensation network, whenever possible, to minimize loading.
- Make sure that the maximum common-mode input-voltage specifications will not be exceeded in the system.
- Decouple the power supply voltages as close to the circuit package as possible.
- Try to separate in-phase inputs and outputs, whenever possible, when preparing the circuit design layout.
- Consult the manufacturer's application notes for additional precautions that are peculiar to the particular circuit being used.

SECTION V

MONOLITHIC MICROCIRCUIT PACKAGES

A. THE PACKAGING OF A MICROCIRCUIT

1. General

The electronic industry has made tremendous advances in semiconductor technology since the development of monolithic microcircuits. The difficulty of capitalizing on the small size of the monolithic silicon dice or bar has focused attention on one of the major barriers to the full realization of its many advantages—the packaging problem.

The packaging of extremely small circuits has lagged somewhat behind semiconductor fabrication and process technology; however, within the past year, much work has been done in assembling and packaging the individual circuit dice. Since a large portion of the finished cost is in the assembly, testing, and packaging of the device, automatic equipment has been developed to assemble and test microcircuits.

A new package, as well as the circuit contained in the package, has not been entirely proven until after a complete system has been designed, assembled, and tested. Any problems that show up are fed back to the device manufacturer for corrective action. This type of feedback has aided in the development of several types of microcircuit packages with adequate mechanical and environmental characteristics. This discussion will describe the methods used for die attachment and intraconnection of the circuit to the package and will present several microcircuit packages.

2. Basic Assembly Techniques

a. General

The basic assembly techniques used in attaching the monolithic circuit die to the package will be discussed with reference to their application to the various microcircuit packages. As with the monolithic fabrication and process technology, the assembly techniques are changing quite rapidly, and there is a wide variation in the techniques now being used by different manufacturers. Most of the techniques have been developed to increase the yield and decrease the cost of microcircuits; however, much has been done to improve their reliability.

Up to the time the slice is bar-probed, very little handling of the slice is done. During the bar-probe test and assembly procedure, the slices and dice are handled and exposed to open environment. Two of the major reliability concerns have been contamination in the package and scratched metallization. Although there are several cleaning steps during assembly, contamination is still a major reliability consideration. A glass-type protective coating over the slice (except the bonding pads) is being investigated and used by some manufacturers to prevent contamination on the die surface and also to protect the metallization.

After the wafer or slice has been fabricated and tested, as discussed in Section II, the individual circuits are ready to be separated and assembled into packages. The original artwork layout will have included several mils of spacing between the neighboring circuits. The protective glass and SiO_2 layer is normally removed from this spacing between circuits. The act of separation, called "dicing," is accomplished by using a diamond stylus in a scribing process.

b. Separation of Individual Circuits from Wafer

The wafer to be diced is held by a vacuum on a table that is capable of coplanar, translational, and rotational motions. Scribing is accomplished by pulling a diamond stylus point across the wafer to form cleavage channels on the surface between the individual circuit die. The principle involved in this is similar to that used in cutting glass. The scribed wafer is removed from the mounting plate and covered with tissue paper. The wafer is broken along the scribed lines by means of light pressure from a rubber roller. The circuits which have passed the bar-probe test are removed by a vacuum pickup with a teflon-coated tip. Some manufacturers use a magnetic ink to mark the circuits which have not passed the bar-probe test. The broken dice are passed under a magnet to remove the bad circuits. The acceptable circuit dice are cleaned and are then ready to be assembled into a circuit package.

c. Attachment of Circuit Die to Microcircuit Package

The circuit die must be bonded to the header or package. This bond must provide mechanical contact, a thermal path, and either electrical connection or isolation. There are two different methods of bonding or attaching the circuit die to the package. One method, used mainly in the metal flat pack, provides electrical isolation between the circuit substrate and the package. It uses a glass frit to secure the silicon die to the base of the package. A thin layer of frit is deposited in the bottom of the package and the circuit die is placed on top of the frit. The assembly is placed in an oven at approximately 450°C to fuse the die to the package. This method is also used in the glass and ceramic packages when a metal bonding plate is not used.

The other method of attaching the die to the package makes use of a eutectic bonding process. This type of bonding is used throughout the semiconductor industry for attaching transistor die to headers. The process varies between manufacturers, depending on the method used for bonding. The package is heated to approximately 400°C, and it may be surrounded by nitrogen gas to minimize oxidation. After the die is located on the header, the eutectic solder is cooled and the die attachment is completed. At this point the assembly is ready for wire-bonding the circuit die to the package leads.

3. Connection to Internal and External Wire Leads

a. General

The physical size and construction of the microcircuit make it necessary to have some type of connection between the chip and the outside of the package. The basic requirements for the package are multileads, mechanical protection, and a hermetic seal. To decrease the cost, the packages should be capable of being used in automatic testing and assembling equipment.

In the interest of clarity, the following definitions will be applied to monolithic electronic devices:

- Intraconnections are those connections and conductors that exist within a single monolithic electronic device package. Header posts and ribbon leads are excluded.
- Interconnections are those connections and conductors that are external to the monolithic electronic device package.

b. Thermocompression Bonding

(1). General. The process of thermocompression bonding of small wire leads to transistor chips has been in use for several years. Transistor reliability data indicate that the technique is fundamentally compatible with the potential reliability of monolithic microcircuit devices. Although the use of wire leads within the device package is likely to continue for some time, their elimination is highly desirable. Substantial research is being carried on toward this end. Wire leads are expensive. They must be installed manually, one at a time, a factor that adds significantly to the labor costs of the device. In addition, a significant portion of device handling, which is responsible for scratched metallization (an important yield factor in addition to reliability considerations), occurs during lead attachment.

Thermocompression bonding is a type of low temperature brazing; it is performed at about 300°C with 0.001-inch diameter gold or aluminum wire and requires the use of machinery especially developed for the purpose. There are three (3) basic types of thermocompression bonds in use in the industry today: wedge bonding, ball bonding, and stitch bonding.

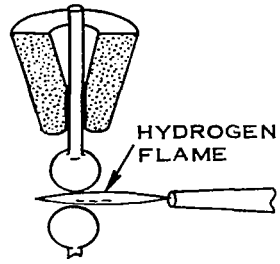
(2). Wedge Bonding. Wedge bonding is simple, inexpensive and does not cause contamination or degradation of the semiconductor. For this process a controlled atmosphere is required. A very fine sapphire or silicon carbide wedge is brought down upon the end of the wire to be bonded. Locally elevated temperatures, coupled with the high pressure, cause the two metals to seize and make intimate contact without a third or intermediate phase (such as solder) and without melting. The function of elevating the temperature is to keep the metals annealed while the pressure is causing them to flow into atomic intimacy.

(3). Ball Bonding. The ball bonding operation, shown in the six-part sequence of Figure 1-89, has the advantage of feeding the wire through the capillary. thus eliminating the need for separate alignment of the parts. The exposed end of the wire is melted into a ball by means of a very small hydrogen flame. This ball is brought down, with pressure, upon the area of contact. Only gold wire can be used in ball bonding; aluminum will not form a suitable ball. Ball bonding usually requires a larger bond area, which results in a very strong bond. The gold wire must be stitch-bonded or wire-welded to the package leads, since a ball cannot be formed at this point.

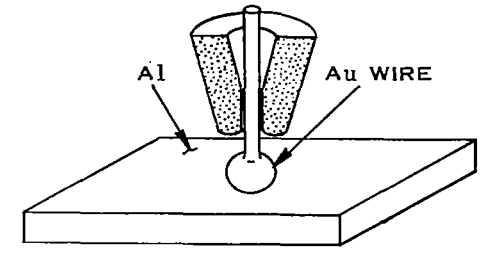
(4). Stitch Bonding. Stitch bonding is a process very similar to ball bonding, in that it uses a capillary action to feed the wire. The exposed end of the wire is bent at an angle of 90° instead of being formed into a ball. The bonding action is then performed with heat and pressure, as in ball bonding. The similarity between stitch bonding and ball bonding is shown in the six-step sequence depicted in Figure 1-90

c. Ultrasonic Bonding

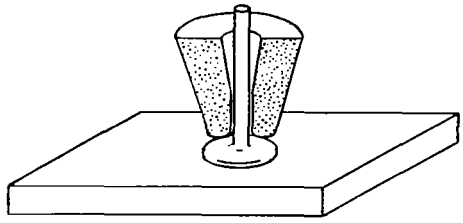
One other type of bonding, recently introduced, shows promise for the future. This is ultrasonic bonding. This method does not make use of an external heat source. The bond is produced by a wiping motion of the ultrasonic head, which causes a plastic deformation of the materials and breaks through any oxide film at the interface between the wire and the bonding pad. Strong intermolecular bonds are formed with large contact areas. This method has the added advantage of using either aluminum or gold wire. The mechanism of ultrasonic bonding is shown in Figure 1-91



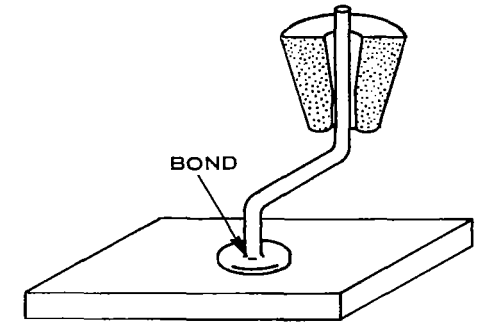
A. BALL FORMING



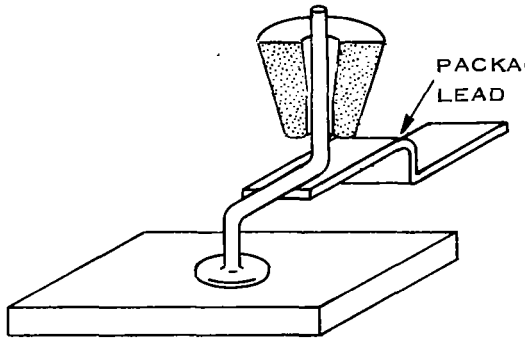
B. ALIGNING BALL ON METAL PAD



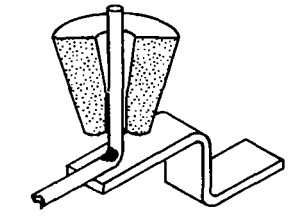
C. EUTECTIC BONDING UNDER THERMAL COMPRESSION



D. POSITIONING AND INDEXING WIRE



E. THERMOCOMPRESSION STITCH BONDING TO PACKAGE LEAD



F. FINISHED INTRACONNECTION

SC08275

Figure 1-89 Thermocompression Ball Bonding

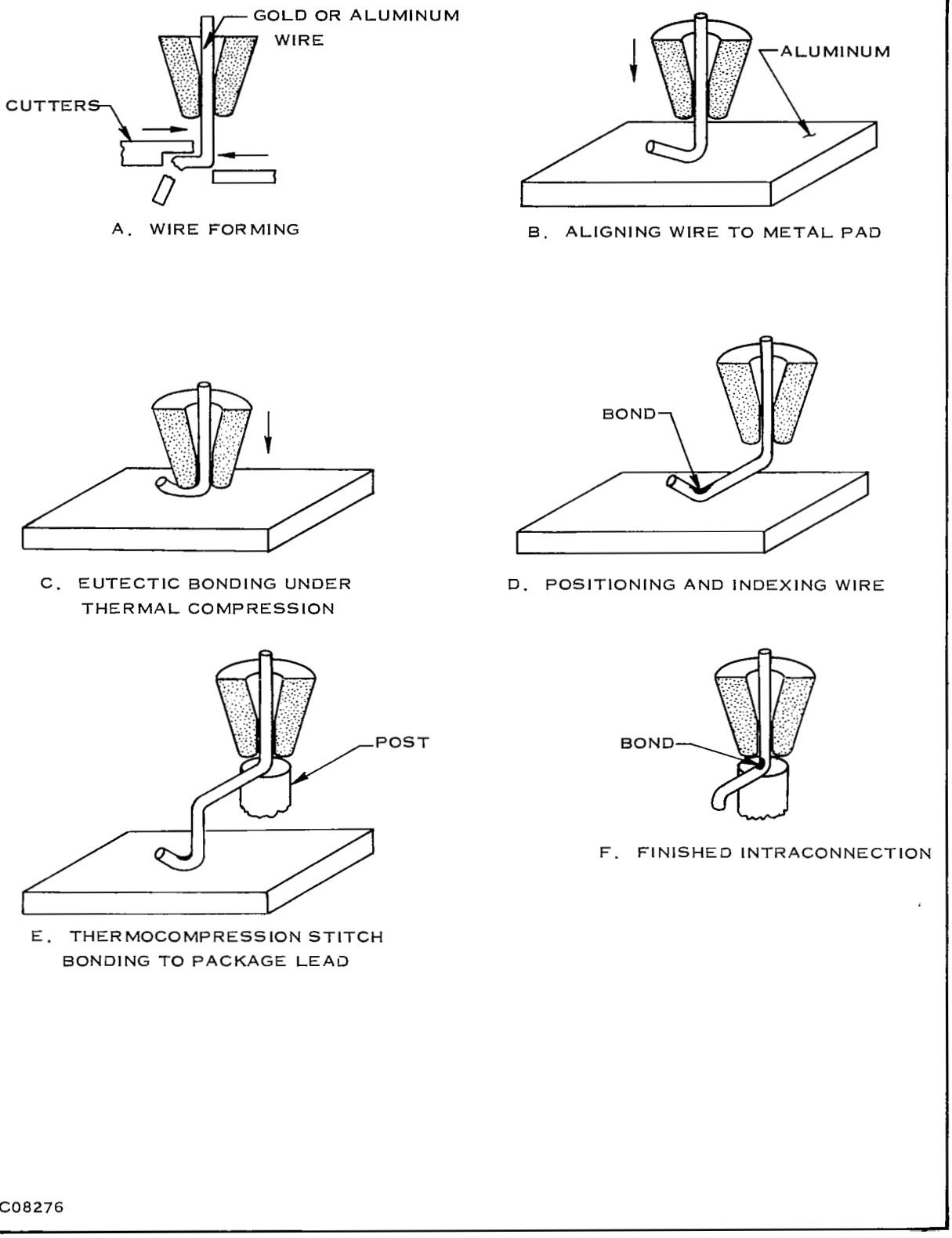


Figure 1-90 Thermocompression Stitch Bonding

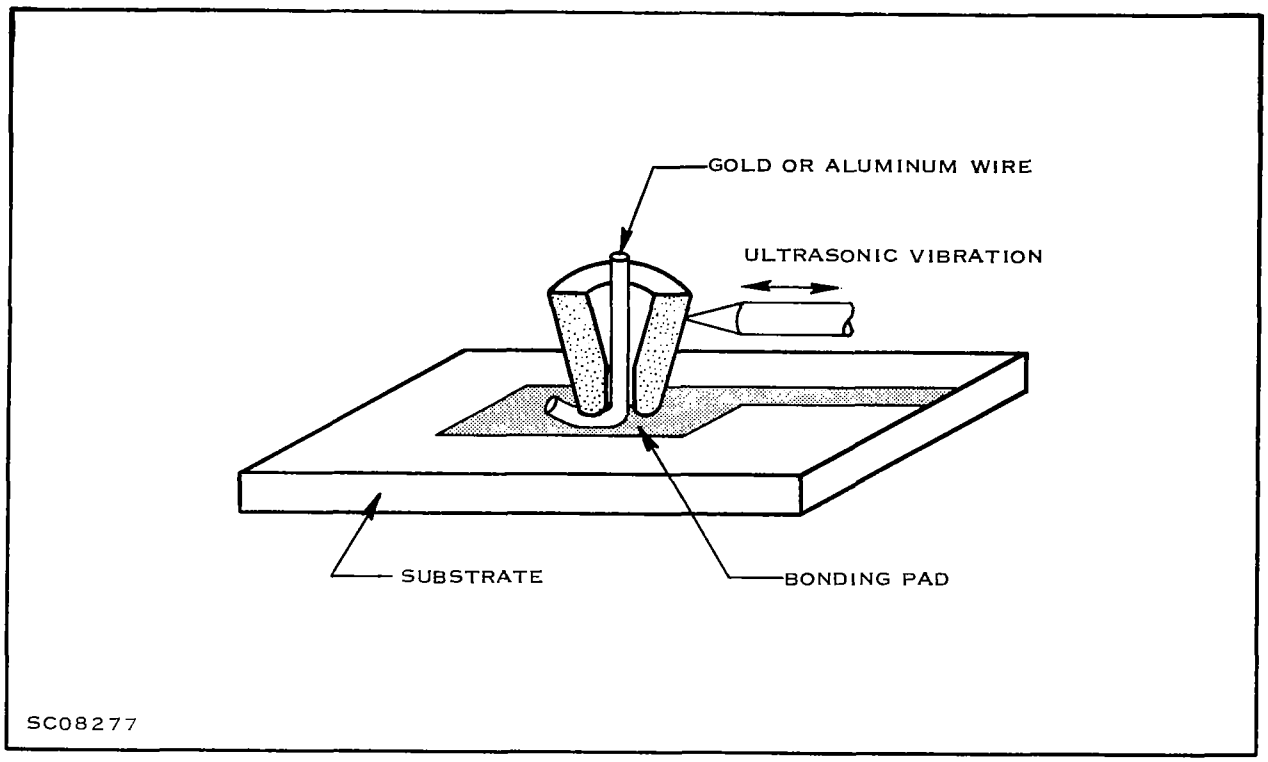


Figure 1-91 Ultrasonic Bonding

4. Flip-Chip Assembly Process

The flip-chip assembly process is an attempt to reduce costs both in the assembly operation and in packaging. It combines the operations of die bonding and wire bonding. In doing this, it eliminates the need for intraconnection wiring. "Flip-chip" gets its name by association with the process procedure. The semiconductor chip or individual component die is coated with a protective glass layer. Holes are etched through the glass to the contact lands, and solder balls (or copper balls) are placed in the holes. Specially prepared substrates are used that have raised metallization lands. The chip is inverted and the balls are pressed against the mating positions on the substrate. This assembly thus provides simultaneous die and intraconnection bonding by means of heat and pressure. It should be possible to extend this technique as experimental data proves its reliability.

B. TYPES OF AVAILABLE PACKAGES

1. General

The packages that are most commonly used can be listed in three different categories: the TO-5* type package, the flat package and the dual-in-line package.

*The designation "TO-5" is a specific JEDEC nomenclature for a three-lead transistor package. The use of the TO-5 name for microcircuit packages with more than three leads is common but is not accurate.

2. The TO-5 Type Package

The first available microcircuit package, the type TO-5, evolved from previous semiconductor technology. This multilead package is available with 8, 10, 12, 14, and even 16 pins. The use of the TO-5 can is shown in Figure 1-92 with a circuit die in the center of the leads. This can, with its cap removed, shows the relative size of the conductors and chip.

The header of the TO-5 type package is made of gold plated F-15 alloy and is fitted with hermetic glass-to-metal seals for the pins. The F-15 alloy is used because of its thermal compatibility with glass and for its weldability. The circuit die is secured on the header and the circuit is intraconnected to larger, more manageable terminals to permit electrical test and operation in its intended application. A nickel-clad cap is welded on the header flange to provide a hermetically sealed package.

There are two major disadvantages to the TO-5 type package. It does not provide sufficient terminals to fully utilize the developing technology of microcircuits unless there is a great sacrifice in packaging space. Secondly, the TO-5 type package is very difficult to use in automatic test and assembly equipment.

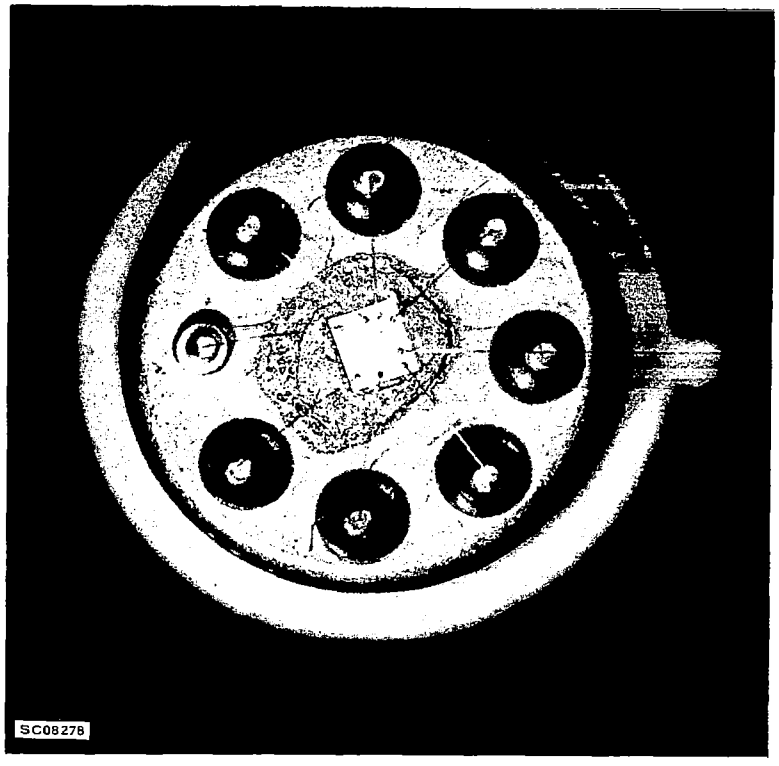


Figure 1-92 View of TO-5 Type Package with Cap Removed

3. The Flat Package

The flat package was developed in order to obtain the full advantage that is available in system packaging for a microcircuit application. The flat pack is usually rectangular or square in design, which makes it compatible with the flat rectangular monolithic die. As with the other elements used in microcircuits, there is little standardization in the flat packs now available from one manufacturer as compared with another. The packages are made from materials such as metal, ceramic, epoxy, glass or combinations of these materials. Three of the commonly used flat packs are shown in Figures 1-93 through 1-98. Although there are perhaps 20 to 30 different size microcircuit flat packs available, the majority of packages use a lead space of 50 mils between leads, which provides a certain degree of interchangeability.

The 14-lead package shown in Figures 1-93 and 1-94 consists of a kovar-stamped ring with slots cut into its sides, a flat F-15 alloy lid (which can be glass-coated to provide protection from shorts to the bond wires) and a baseplate welded to each side of the ring. The leads are gold-plated F-15 glass-sealing alloy (F-15 is the ASTM designation for an iron-nickel-cobalt containing, nominaly 53 percent iron, 24 percent nickel, and 17 percent cobalt). Since the leads are gold-plated, they can be either welded or soldered.

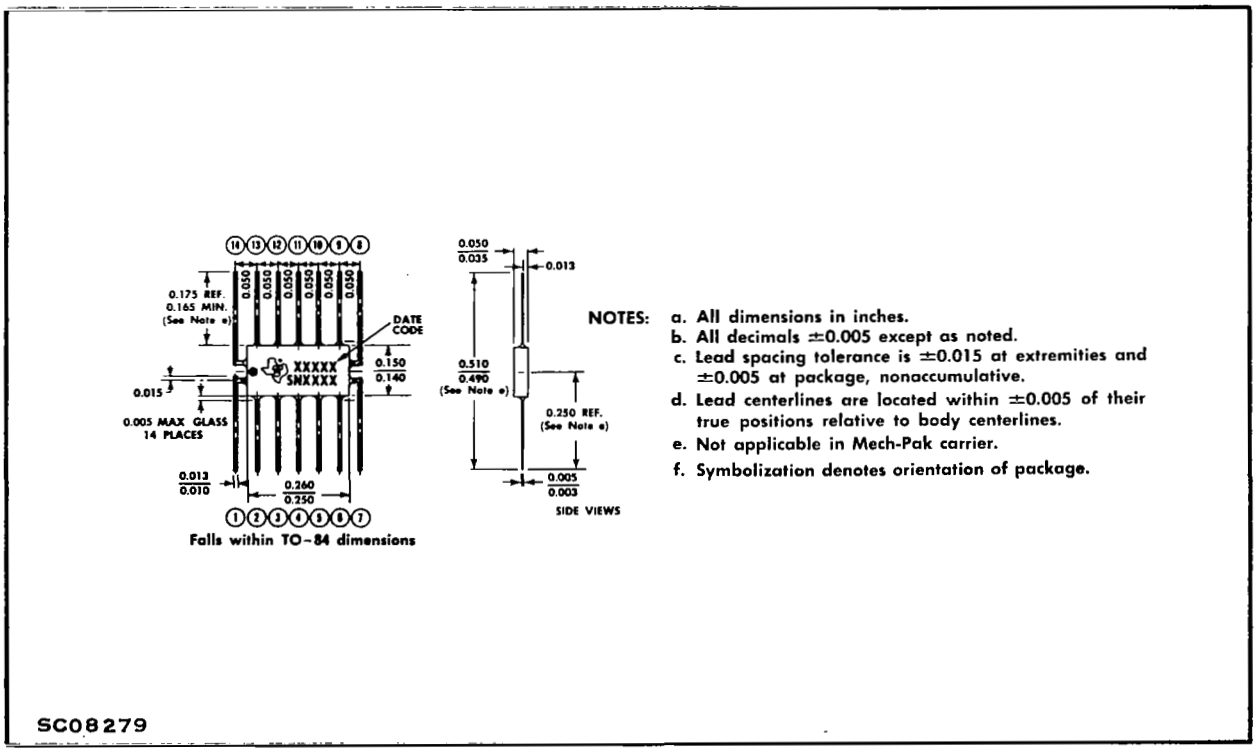


Figure 1-93. Profile and Plan Views of Metal Flat Pack (Texas Instruments)

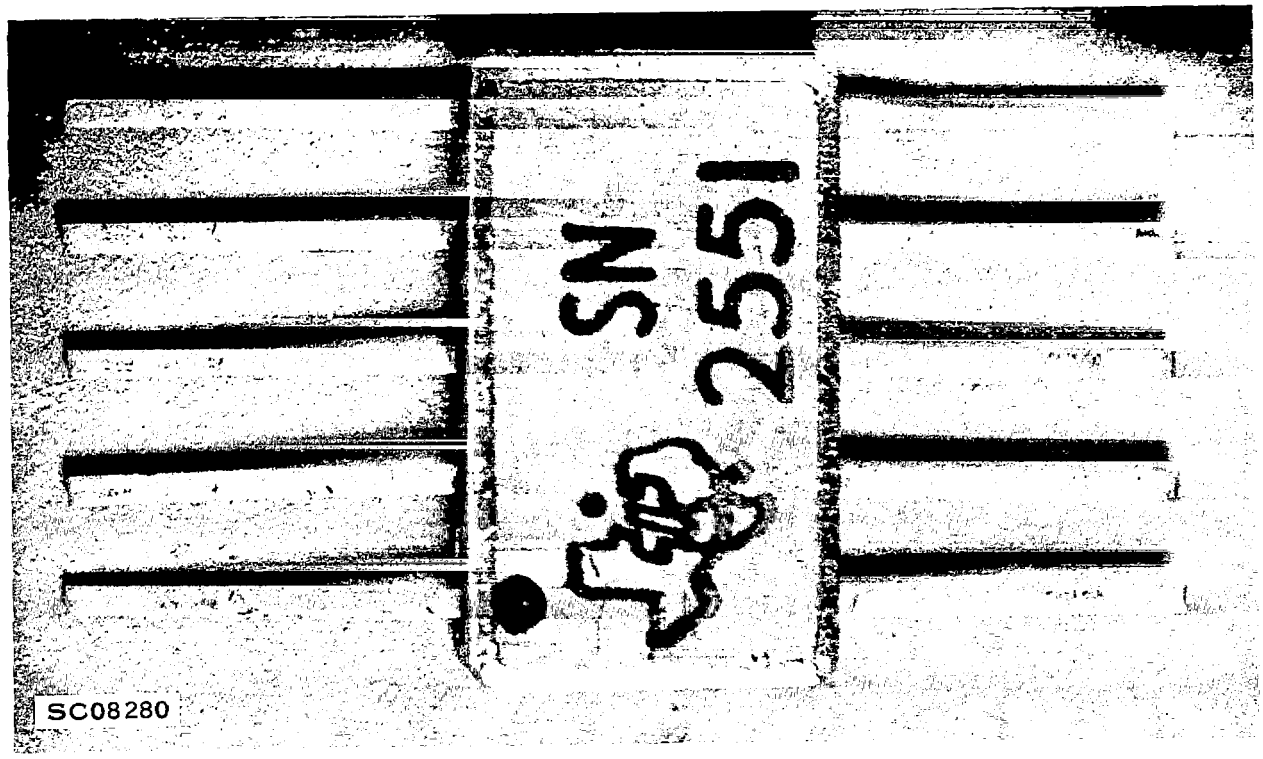


Figure 1-94 Photograph of Metal Flat Pack (Texas Instruments)

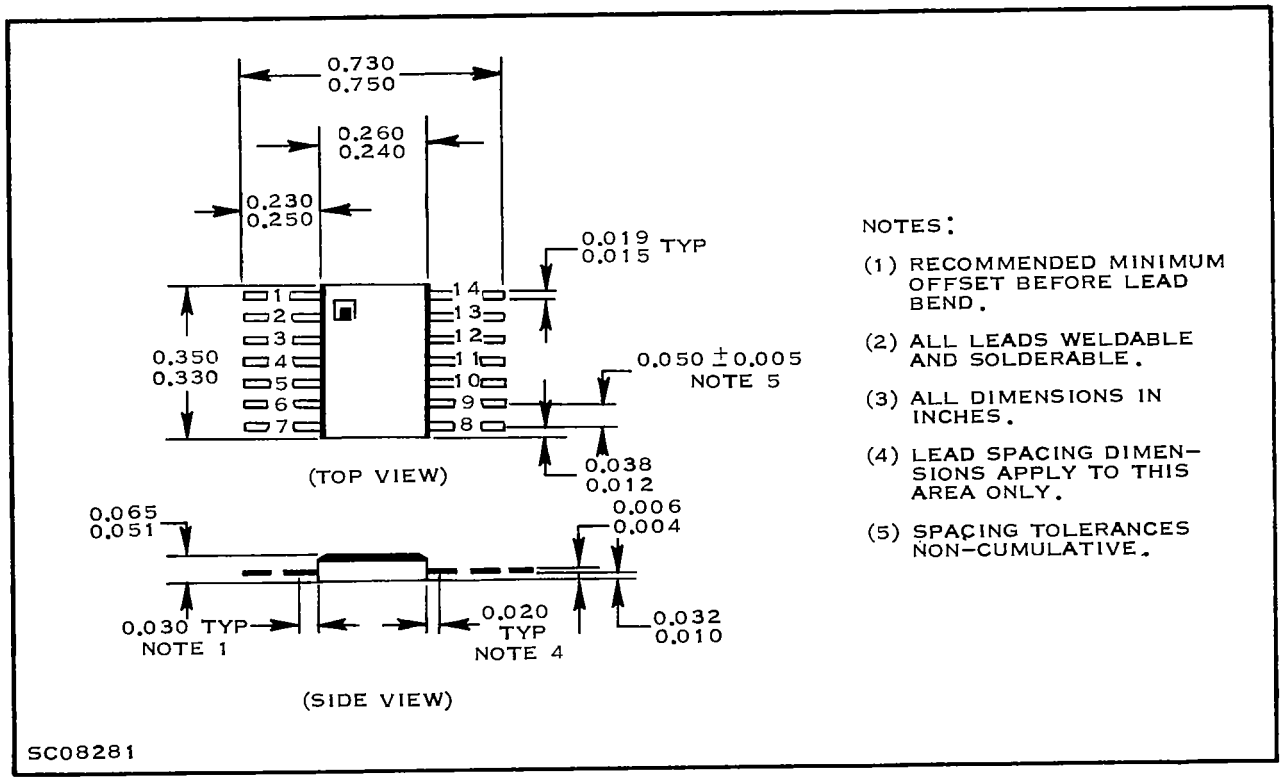


Figure 1-95 Plan View of Glass - Metal Flat Pack (Signetics)

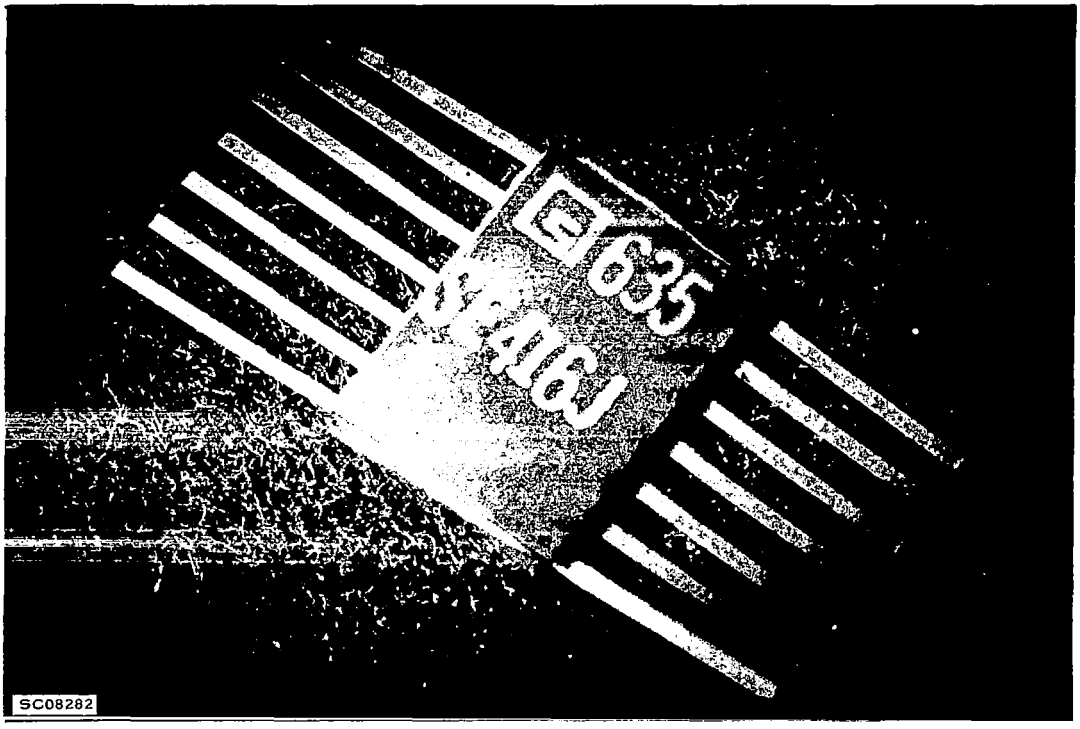


Figure 1-96. Photograph of Glass - Metal Flat Pack (Signetics)

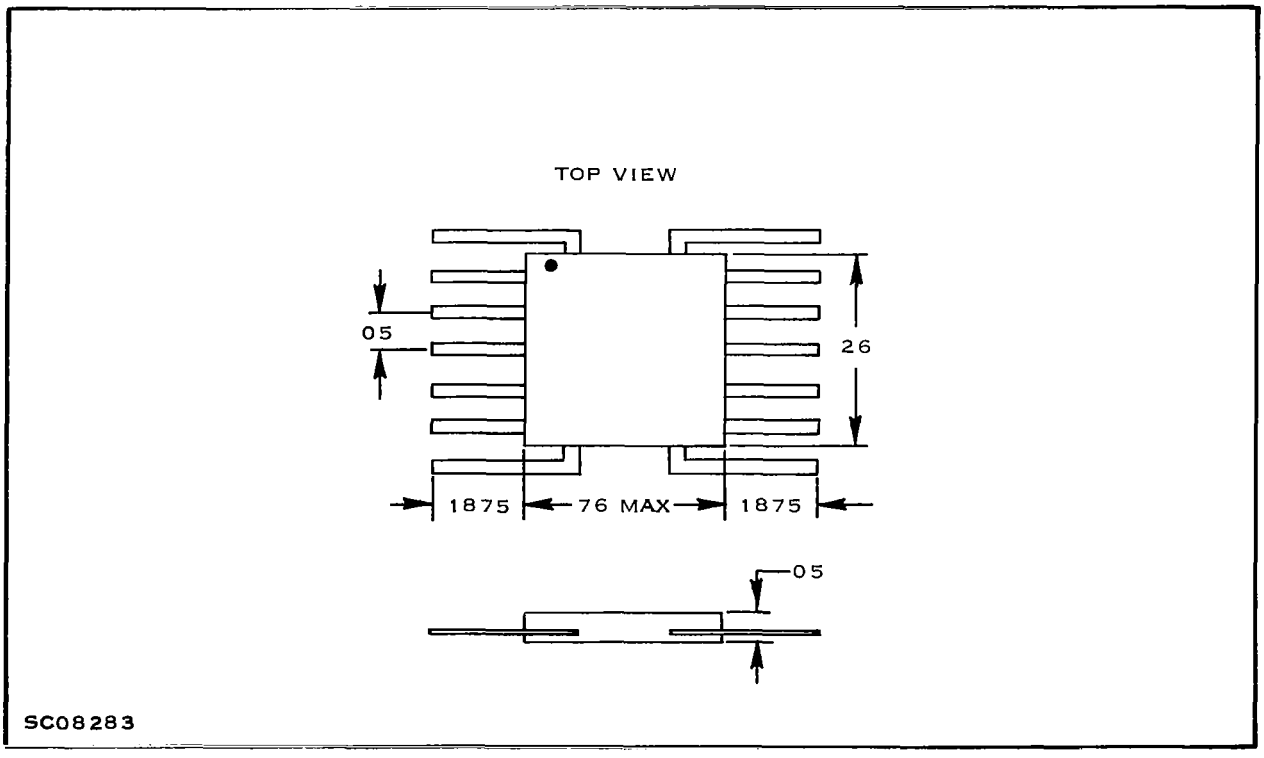


Figure 1-97. Plan View of Ceramic Flat Pack (Fairchild)

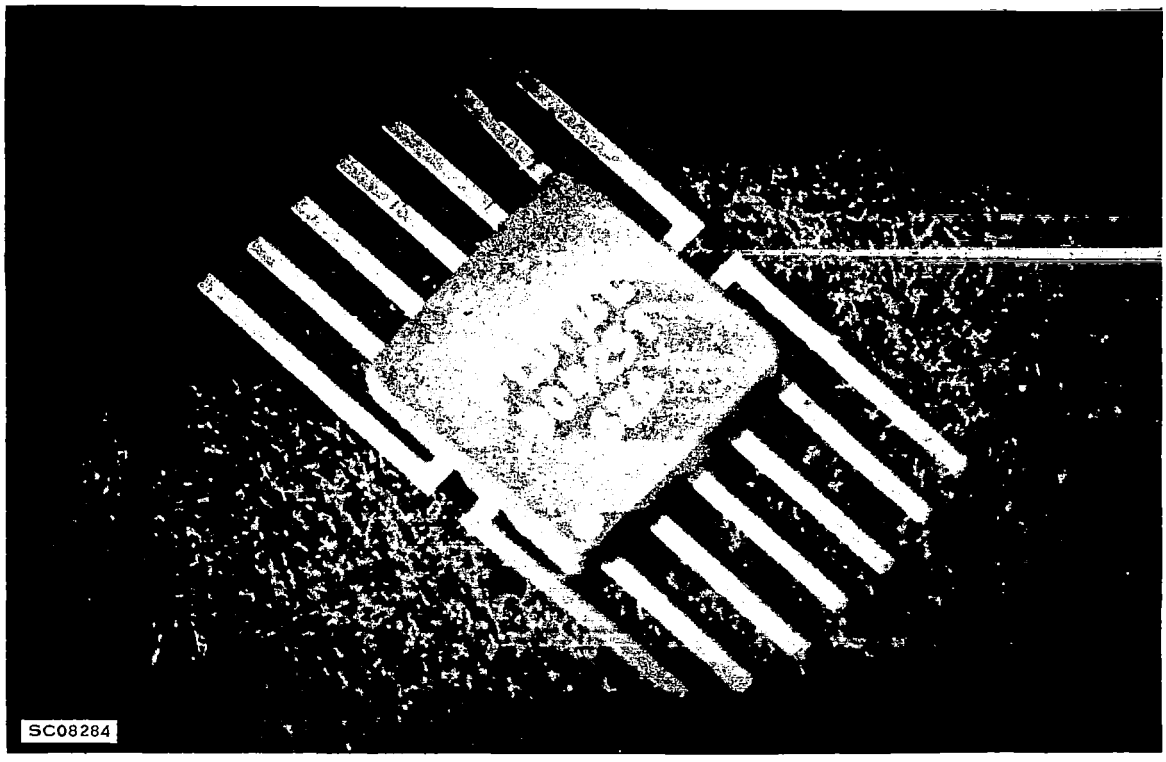


Figure 1-98 Photograph of Ceramic Flat Pack (Fairchild)

The package shown in Figures 1-90 and 1-91 is an all-glass body with a Kovar lid. The leads are sealed within the glass mounting base. One of the leads continues on the inside to a mounting plate for the circuit die. A glass frit is used to bond the lid to the glass body.

Another flat package, shown in Figures 1-92 and 1-93, is constructed completely of ceramic, with gold plated F-15 alloy leads. As with the glass package, a gold preform is used for bonding the circuit die to the package. A glass solder is used to seal the ceramic lid to the body.

4. Dual-In-Line Package

One other enclosure, the dual-in-line (DIP) package, has attained a market recently. Shown in Figure 1-99 is the dual-in-line (DIP) package used in commercial applications. The DIP is made by two different concepts. One method uses a ceramic substrate and cap, with a glass frit to bond the two together and to provide the seal at the leads. The other method uses an epoxy for the body of the DIP. This provides an economical package, but it is not hermetically sealed, and the reliability of such a package has not yet been fully established.

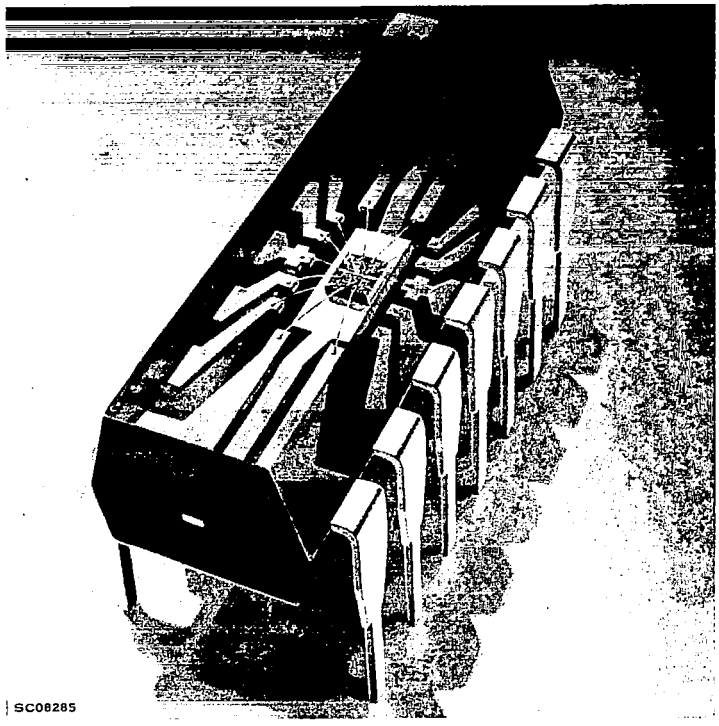


Figure 1-99 Photograph of Dual-In-Line Package (Texas Instruments)

The DIP package was designed to accomodate standard commercial assembly methods, particularly those used by commercial computer manufacturers. The physical size and terminal dimensions are standard with most manufacturers; however, as brought out before, very few manufacturers have identical circuits available within the package.

C. SELECTING A PACKAGE

1. General

There are no hard and fast rules for selecting a microcircuit package. For military applications, only two types of packages are now being used, the TO-5 type, and the flat pack. Package selection has been given low priority when choosing,a microcircuit family. The reason for this is that when a family is chosen, the system manufacturer is usually limited to one source and must accept the device manufacturer's "unique" package. This will continue to be the case for several years, until second sources are available for the same circuit and until some standardization is achieved between device manufacturers.

2. The TO-5 Package

The TO-5 type package and a majority of the flat packs now available are capable of meeting the requirements for military and space equipment. There have been sufficient reliability data and system data on these packages to justify their use in the majority of applications. The TO-5 package has an advantage in that its system assembly procedure is well known, due to the use of transistors. It also provides better thermal characteristics than the flat pack.

3. The Flat Package

The concept of the flat package, established in 1959, has enhanced the utility of the semiconductor circuits. This package-form factor, with its multiple leads, is essential for today's multifunction digital semiconductor circuits. The weight of the package is generally very low, less than 0.1 gram. The mechanical strength of the metal-to-glass construction and a low mass enable the flat pack to withstand severe stresses and environmental conditions. The leads on the flat pack make it adaptable to printed circuit board layout. The lateral extension of the leads allows mounting by either welding or soldering. The leads should be preformed, as shown in Figures and 1-96, to provide a more reliable assembly. The formed leads will help to prevent cracks in the seal around the leads. Also, the flat pack provides stress relief for the seal during extreme environmental conditions.

Special carriers are needed for handling and testing flat packs. This does provide some plus factors, because the carriers can be keyed for automatic orientation and stacked for automatic placement on boards. These carriers also prevent damage during shipping and handling. A microcircuit in a meck-pack carrier is shown in Figure 1-100.

D. PACKAGE ASSEMBLY AT THE SYSTEM LEVEL

1. General

For the packaging engineer to adequately utilize the factors presented to him by a microcircuit, he must carefully examine the design. The higher the density of the package the more thought and effort will be required for proper thermal control and isolation of signals. Since the optimization of every electrical and mechanical characteristic of the package is impossible, a design-compromise principle must be used to optimize the desirable features and minimize the trade-offs necessary to secure it. There are no magic rules of thumb to guide the packaging engineer through the maze of requirements. Each new microcircuit design will have different problems than the last.

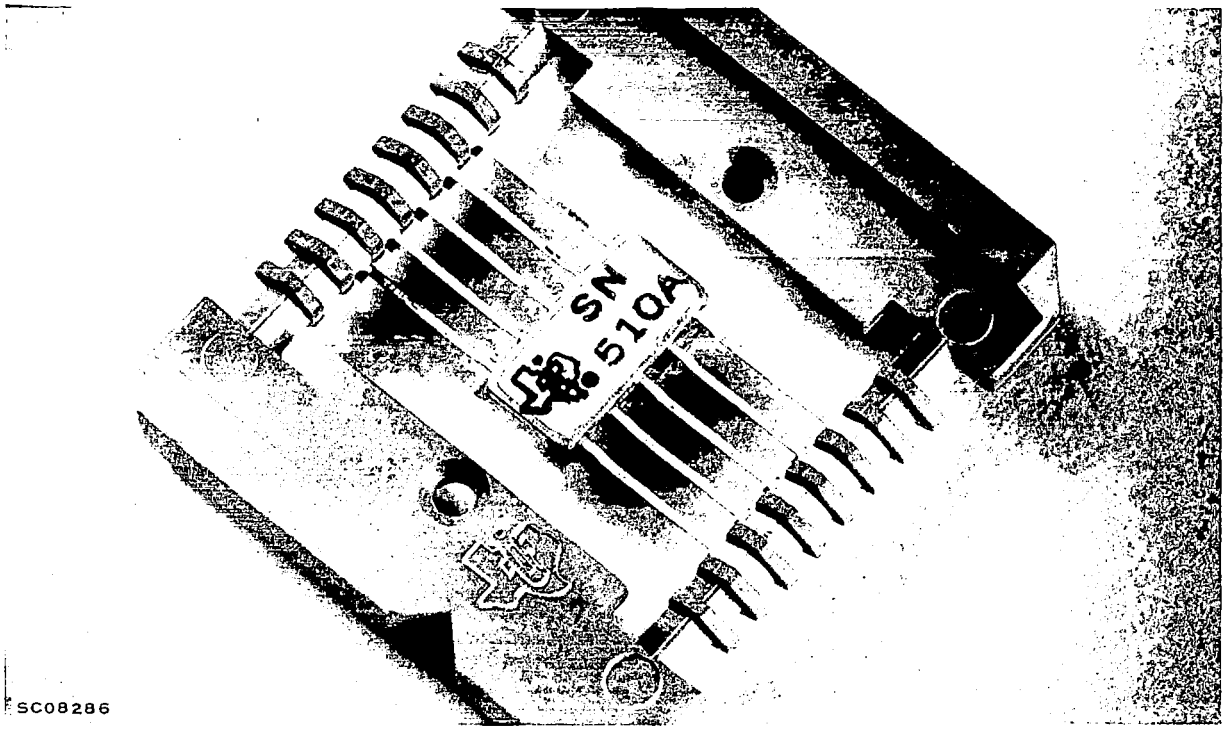


Figure 1-100. Microcircuit Mech - Pack Carrier

2. System Integration

a. The TO-5 Package

The TO-5 package can be assembled in a system by using the flow solder technique. This technique, widely used in industrial and consumer applications, has been the main reason for the popularity of the TO-5 package.

b. The Flat Package

(1). General. A different technique is used for attaching the flat pack to printed circuit (PC) boards. The most common methods for adjoining the flat pack leads to printed circuit boards are resistance-parallel-gap welding and reflow soldering.

(2). Resistance Welding. Resistance welding is so named because, while force is applied to the materials to be welded together, low-voltage, high-current energy is passed through the resistance of the materials. The contact area is very small, resulting in a very-high-current density area, which causes plastic deformation. The materials are "pushed" together by the force of the electrodes. A nugget or fusion weld is not obtained, as in arc welding instead, a molecular bond is achieved.

Although a molecular bond provides a very reliable connection, there are two definite disadvantages, the first being that maintainability is limited (usually only one repair can be made per circuit). The other disadvantage is that resistance welding is expensive and is not suited for automated assembly (nickel-plated circuit boards must be used).

(3). Reflow Soldering. Another method being investigated and used for attaching flat packs to circuit boards is reflow soldering. The leads on the microcircuit device and the pattern on the circuit board are solder coated. The device is positioned on the board and heat is applied to melt the solder and secure the microcircuit to the circuit board. One type of reflow soldering is also known as hot-gas soldering. It is accomplished by passing a stream of nitrogen gas over a hot coil of nichrome wire which is encased in a tube. The tube has an integrated nozzle which directs the hot gas at the joints to be soldered. There is no flame present. Gas in the tube is heated to approximately 900°F. The hot gas strikes the solder joints on the PC board at a temperature in the range of 600°F to 650°F. The gas flow rate is approximately 1.5 cu. ft./hr. Thus a solder joint can be made in the time of two or three seconds, which minimizes the possibility of heat damage to the component. The main advantage of this method is that it makes it possible to design the heating apparatus to solder all the leads on the device simultaneously, in the two- or three-second span. Also, the reflow solder process uses conventional copper circuit boards.

c. Dual-In-Line Package

The new DIP package can be attached by the flow solder process, and the package can be automatically inserted in the circuit boards.

SECTION VI

THE EFFECT OF MICROCIRCUITS UPON SYSTEM RELIABILITY

It is common knowledge throughout the electronic industry that system reliability has a direct bearing upon mission success, system operating life, system maintenance costs, system availability, and program development costs. Also, it is known that the total system reliability is a function of the total number of parts contained in the system and the reliability of each individual part. The overall system reliability can be improved by reducing the number of parts and improving the reliability of the individual parts. A significant effect on system reliability has been realized through the use of microcircuits.

System reliability improvements are not only due to the reduction of component count but also to the following factors:

- The problem of parts standardization and control is minimized.
- The reliability problems associated with incorrect application are reduced, since microcircuits are designed to function under very specific conditions.
- The use of microcircuits requires less control on stress levels and derating rules when the system is operated at recommended conditions.
- The use of microcircuits has greatly reduced the number and types of circuit connections. A large portion of the connections are the intraconnections of components within the microcircuit package. Thus, the component connections on the printed circuit board have been reduced; however, the system connector problems (PCB connectors) are sometimes complicated due to the decrease in the system size.

Many factors must be considered in order to obtain the necessary reliability of a system. They range from selection of the right devices and computation of the right failure rate, through specifications, conditioning of parts, and determination of application rules, system design, and assembly.

One must choose microcircuits that will provide the reliability required for the system. Reliability is built into the circuit as it is fabricated and assembled. One

cannot screen and condition just any circuit and consistently achieve a high degree of reliability. Process control is the main factor in achieving a reliable device. Thus, when choosing a family of microcircuits or a manufacturer, investigation of the fabrication processes and techniques used in production is of the utmost importance.

Nearly every project and proposal having a reliability requirement must predict and sometimes formally demonstrate a certain MTBF. It is therefore important that a realistic (obtainable) failure rate be used for microcircuits.

A definite advantage of microcircuits is their low failure rate. The failure rate is comparable to the failure rate of a discrete transistor. Therefore, in comparing the failure of a monolithic device to the failure rate of an equivalent circuit using discrete components, a reduction in the failure rate of up to two orders of magnitude has been observed and demonstrated. The failure rate of microcircuits is becoming extremely low due to gains in technical knowledge by both the manufacturer and the user, and to better processes and better control of these processes. Demonstrated failure rates have consistently equaled those of silicon planar resistors.

Extreme caution will be necessary in deriving a valid failure rate number. In a recent survey of available tests and operational data from microcircuit manufacturers and users, failure rates ranging from 0.001 failure per million hours to 1.0 failure per million hours were observed. These failure rates were primarily dependent upon the processing, inspection, and manufacturing controls used by the manufacturer, and upon the screening and preconditioning tests performed by the manufacturer or user. Different manufacturers use different methods and tests in obtaining failure rates, hence the wide range of failure-rate numbers. It is difficult to compare these numbers and it is more difficult to obtain an overall failure rate unless the test methods, failure criteria, and types of microcircuits are known.

This volume of the Handbook has presented application information needed to achieve high reliability in a system using microcircuits. The other volumes present information on failure mechanisms, failure analysis methods and procedures, and reliability assessment. The system design and reliability engineer must assimilate this information, evaluating it as to the degree it applies to a specific system or piece of equipment.

APPENDIX A

TYPICAL DATA SHEETS FROM VARIOUS MANUFACTURERS

μA711
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar epitaxial process.

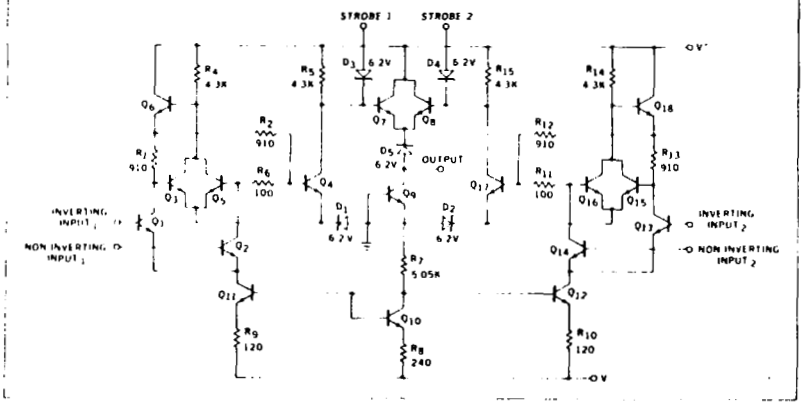
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55 C to +125 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature (Soldering, 60 sec.)	300 C

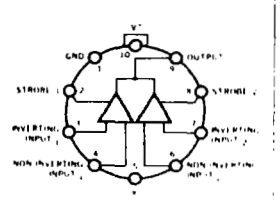
PHYSICAL DIMENSIONS

ORDER PART NO
U5F771131x

SCHEMATIC DIAGRAM



TO-5 CONNECTION DIAGRAM (TOP VIEW)



Notes on page 2

SC10997 (1-4)

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U.S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117760. OTHER PATENTS PENDING

Figure A-1. Fairchild μA711 (Sheet 1 of 4)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	3.5	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	5.0	mV
Input Offset Current	V_{out} = +1.4 V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		nsec
Strobe Release Time			12		nsec
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 0		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for -55°C $\leq T_A \leq$ +125°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, V_{CM} = 0			4.5	mV
	$R_S \leq 200\,\Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

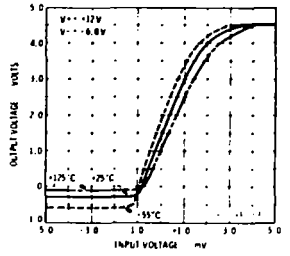
(3) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

SC10997 (2-4)

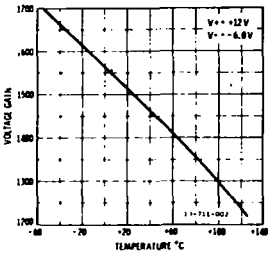
Figure A-2. Fairchild μA711 (Sheet 2 of 4)

TYPICAL ELECTRICAL CHARACTERISTICS

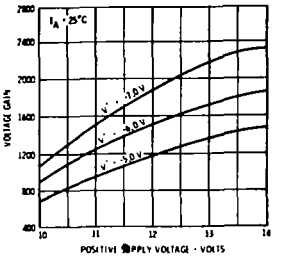
VOLTAGE TRANSFER CHARACTERISTIC



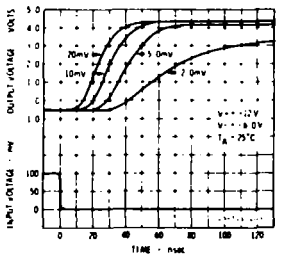
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



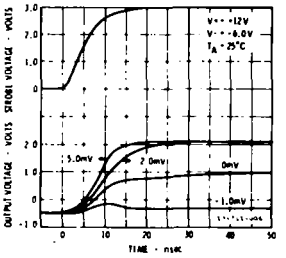
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



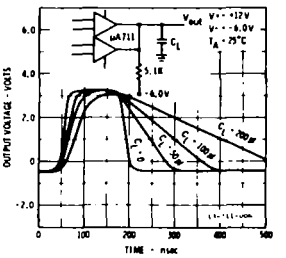
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



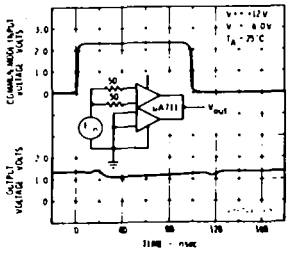
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



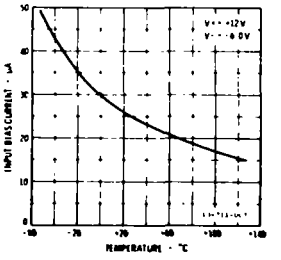
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



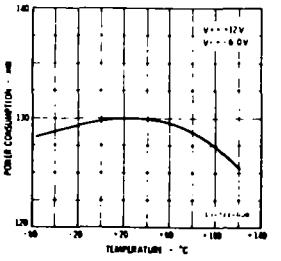
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



SC10997 (3-4)

Figure A-3. Fairchild μA711 (Sheet 3 of 4)

DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

SC10997 (4-4)

Figure A-4. Fairchild μA711 (Sheet 4 of 4)

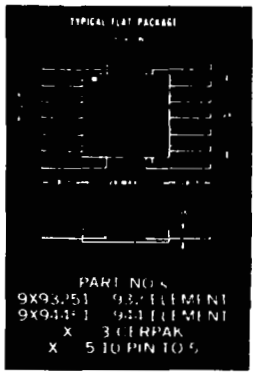
DTμL 932 DUAL BUFFER ELEMENT
DTμL 944 DUAL POWER GATE ELEMENT
FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

GENERAL DESCRIPTION - The DTμL 932 Dual Buffer Element and the DTμL 944 Dual Power Gate Element are dual 4-input inverting drivers for use with the Fairchild Diode-Transistor Micrologic Family or any similar DTL logic circuits. The fan-in of either element may be extended with the use of the DTμL 933 Element. Input thresholds and currents are the same as other DTμL gate elements.

Both DTμL 932 and DTμL 944 Elements have typical saturation resistances of 5 ohms which allow output currents of up to 100 mA. The DTμL 932 features an emitter-follower output pull-up, which provides a high fan-out device with superior capacitance-driving capability.

The DTμL 944 features an output with no internal pull-up. Thus, 944 outputs may be tied together for the "wired-OR" function, or may drive inputs with logic thresholds of 4 to 6 volts. The 944 is intended as a high fan-out gate interface driver, or low-power lamp driver. An external pull-up resistor may return to the nominal DTμL V_{CC} supply of 5 volts or to other supplies up to 12 volts. These supplies may be located near the output or at the far end of an open transmission line or twisted pair interconnection.

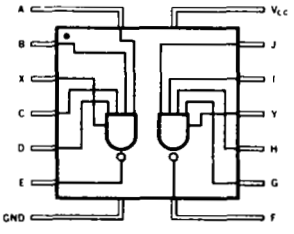
Complete test specifications, typical and worst-case DC curves, t_{pd} curves, and suggested loading rules are included in these specifications.



ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Supply Voltage (V_{CC}), -55 C to +125 C, Continuous	+8.0 Volts	Input Reverse Current	5.0 mA
Supply Voltage (V_{CC}), pulsed, 1.0 sec.	+12 Volts	Operating Ambient Temperature	-55 C to +125 C
Output Current, into Outputs, Continuous	150 mA	Storage Temperature	-65 C to +150 C
Output Current, into Outputs, pulsed, 30 milliseconds	300 mA	Operating Junction Temperature (See note A on page 2)	+175 C Maximum
Input Forward Current	-10 mA		

LOGIC DIAGRAM (TOP VIEW)



POSITIVE (NAND) LOGIC

$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

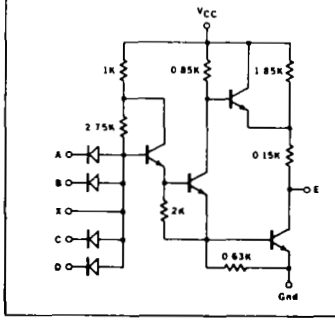
$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

NEGATIVE (NOR LOGIC (symbol not shown)

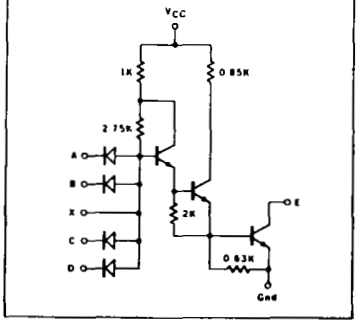
$E = \overline{A + B + C + D + (X)}$

$F = \overline{G + H + I + J + (Y)}$

SCHEMATIC DIAGRAM OF THE DTμL 932 ELEMENT (ONE SIDE ONLY)



SCHEMATIC DIAGRAM OF THE DTμL 944 ELEMENT (ONE SIDE ONLY)



SC08853 (1-4)

MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3025589, 3064167, 3108359, 3117260. OTHER PATENTS PENDING

Figure A-5. Fairchild DTμL 932 and DTμL 944 (Sheet 1 of 4)

FAIRCHILD DIODE-TRANSISTOR MICROLOGIC

TEST SEQUENCE DTμL 932 AND DTμL 944 ELEMENTS

NOTE: Both elements are dual "NAND" gates, therefore, the test sequences for each are identical. Tests on each side of the dual are identical, therefore, matching test and pin numbers are shown in parentheses.

Test No.	LTPD Group	Notes	Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	Limits Min.	Limits Max.
1, (2)	A		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	$V_E(V_F)$		V_{OL}
3, 4, 5, 6, (7, 8, 9, 10)	B	1, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
11, (12)	C		V_R	GND	GND	GND			V_{CCH}	$I_A(I_G)$		I_R
13, (14)	C		GND	V_R	GND	GND			V_{CCH}	$I_B(I_H)$		I_R
15, (16)	C		GND	GND	V_R	GND			V_{CCH}	$I_C(I_I)$		I_R
17, (18)	C		GND	GND	GND	V_R			V_{CCH}	$I_D(I_J)$		I_R
19, (20)	D		V_F	V_R	V_R	V_R			V_{CCH}	$I_A(I_G$		I_F
21, (22)	D		V_R	V_F	V_R	V_R			V_{CCH}	$I_B(I_H)$		I_F
23, (24)	D		V_R	V_R	V_F	V_R			V_{CCH}	$I_C(I_I)$		I_F
25, (26)	D		V_R	V_R	V_R	V_F			V_{CCH}	$I_D(I_J)$		I_F
27, (28)	C	3	GND					V_{CEX}	V_{CEX}	$I_E(I_F)$		I_{CEX}
29, (30)	B	2, 3	GND					GND	V_{CCH}	$I_E(I_F)$	I_{SC}	
31	E								V_{PD}	I_{VCC}		I_{PDH}
32	E	2	GND						$V_{(max)}$	I_{VCC}		$I_{(max)}$
33, (34)	E	3					V_X	I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
35, 36	F	t_{pd+}, t_{pd-} See Table of test circuit conditions and limits.										
35, 36, 37, 38 (39, 40, 41, 42)	B	1, 4	V_{IL}	V_{IL}	V_{IL}	V_{IL}		V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
43, (44)	B	4					V_X	V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
45, (46)	B	4	GND					I_{CE}	V_{CCH}	$V_E(V_F)$	LV_{CE}	

NOTES:

(1) V_{IL} applied individually to 1 input each test. Other inputs open

(2) Apply GND to both pins A and G.

(3) DT L 932 only.

(4) DT L 944 only.

(5) On 10 Pin TO 5 units, pins D, X, I and J are omitted. Thus tests 6, 9, 10, 16, 17, 18, 24, 25, 26, 33, 38, 41, 42 and 43 do not apply

TEST LIMITS—DTμL 932 AND DTμL 944

	Units	-55 C Min	-55 C Max	+25 C Min	+25 C Max	+125 C Min	+125 C Max
V_{OL}	Volts		0.4		0.4		0.45
V_{OH}	Volts	2.6		2.5		2.5	
I_R	μA		2.0		2.0		5.0
I_F	mA		-1.6		-1.6		-1.5
I_{CEX} 932	μA		50				
I_{SC} (min) 932	mA	-16		-18		-16	
$I_{(max)}$ 932&944	mA				6.0		
I_{PDH} 944	mA				20		
I_{PDH} 932	mA				26.6		
I_{CEX} 944	mA		0.05		0.1		0.2
LV_{CE} 944	Volts				6.0		

CONDITIONS AND LIMITS, t_{pd} TESTS

(V_{CC} = 5.0 V, T_A = 25 C)

		R	C	Min.	Max.	
t_{pd+}	944	510 Ω	20 pf	15 nsec	50 nsec	
t_{pd-}	944	150 Ω	100 pf	10 nsec	35 nsec	
t_{pd+}	932	510 Ω	500 pf	25 nsec	80 nsec	
t_{pd-}	932	150 Ω	500 pf	15 nsec	40 nsec	
t_{pd+}	944	150 Ω	20 pf	10 nsec	35 nsec	(Note 1)
t_{pd-}	944	510 Ω	20 pf	5.0 nsec	20 nsec	(Note 1)
t_{pd+}	932	150 Ω	500 pf	20 nsec	65 nsec	(Note 1)
t_{pd-}	932	510 Ω	200 pf	8.0 nsec	30 nsec	(Note 1)

NOTE: Correlating limit provided as design information only

FORCING CONDITIONS

	Units	-55 C	+25 C	+125 C
$V_{(max)}$	Volts	--	8.0	--
V_{PD}	Volts	--	5.0	--
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_R	Volts	4.0	4.0	4.0
V_F	Volts	0	0	0
V_{CEX}	Volts	4.5	4.5	4.5

	Units	-55 C	+25 C	+125 C
I_{OL} 944	mA	36	40	36
I_{OL} 932	mA	34	36	32
I_{OH} 932	mA	-2.0	-2.5	-4.0
V_{IL}	Volts	1.4	1.1	0.8
V_{IH}	Volts	2.1	1.9	1.7
V_X	Volts		1.8	
I_{CE} 944	mA		5.0	

NOTE A:

Allow 200 C Watt θ_{J-A} for TO-5, 300 C Watt θ_{J-A} for cerpak. Allow 50 C Watt θ_{J-C} for TO-5, 180 C Watt θ_{J-C} for cerpak. Heat removal in cerpak is highly dependent upon contact surfaces or air flow and on lead attachment and Thermal paths thru leads, as well as number of soldered leads.

SC08853 (2-4)

Figure A-6. Fairchild DTμL 932 and DTμL 944 (Sheet 2 of 4)

MINIMUM/MAXIMUM AND TYPICAL DC CURVES

FIG. 1. −1 I, DTμL932, 944 MAXIMUM VS. TYPICAL (T_A = −55°C & +25°C)

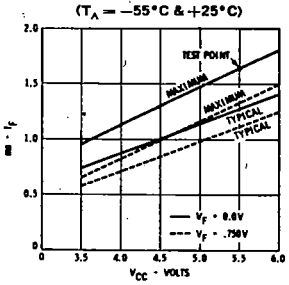


FIG. 2. DTμL INPUT THRESHOLDS VS. TEMPERATURE (932, 944)

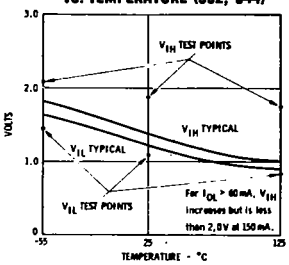


FIG. 3. TYPICAL POWER DISSIPATION PER SIDE VS. SUPPLY VOLTAGE (OUTPUT NOT LOADED) (932, 944)

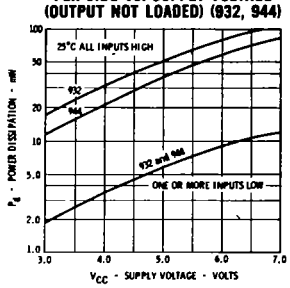


FIG. 4. TYPICAL OUTPUT CURRENT WITH INPUTS LOW (932)

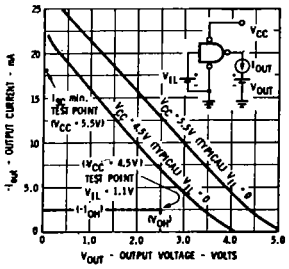


FIG. 5. TYPICAL OUTPUT LOW CURRENT VS. SUPPLY VOLTAGE (−55°C and +25°C) (932)

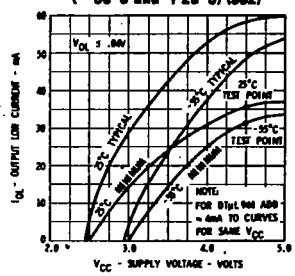


FIG. 6. TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (932)

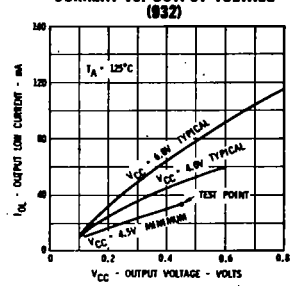
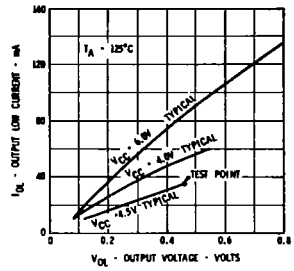


FIG. 7. TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE (944)



t_{pd} CURVES

FIG. 8. TYPICAL t_{pd}− VS. CAPACITY (932, 944)

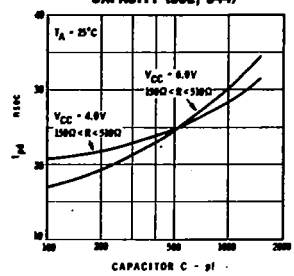


FIG. 9. TYPICAL t_{pd}+ VS. CAPACITY (944)

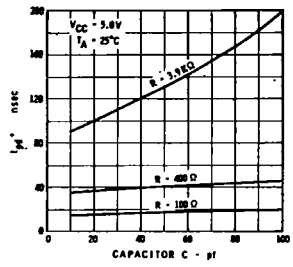
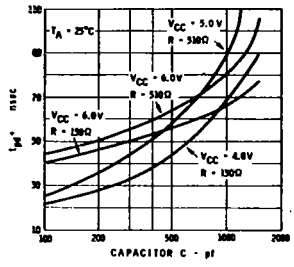
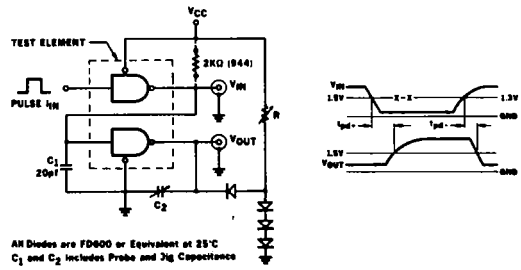


FIG. 10. TYPICAL t_{pd}+ VS. CAPACITY (932)



t_{pd} TEST CIRCUIT FOR DTμL 932 ELEMENT

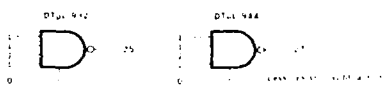


NOTE:
The same circuit is used on the DTμL 944 element except that all diodes are omitted. The resistor R is tied to capacitor C and the Test Output. A 2KΩ resistor is used to load the input gate.

SC08853 (3-4)

Figure A-7. Fairchild DTμL 932 and DTμL 944 (Sheet 3 of 4)

SUGGESTED INPUT-OUTPUT LOADING FACTORS (Please refer to DTμL Composite Data Sheet for complete family rules).



INPUT LOAD FACTORS FOR OTHER DTμL ELEMENTS

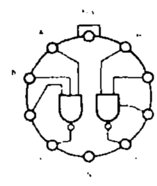
1 DTμL 930, 946, 932, 944 inputs
2 DTμL 931, 945, 948 CP pin
2/3 DTμL 931, 945, 948 S_1 S_2 C_1 C_2
3/4 DTμL 931 S_D C_D pins
2 DTμL 945, 948 S_D C_D pins
[illegible] DTμL 9103, 9104 which drives DTμL 932 or 944 with external resistor 510Ω

MISCELLANEOUS RULES

1. DTμL 932 may not be output "OR"ed.
2. For increased current, inputs and outputs of 1/2 DTμL 932 or 1/2 DTμL 944 may be paralleled up to 4 common outputs. Each combined input = 4 loads. Combined output = 100 loads.
3. DTμL 944 may be output "OR"ed.
4. An external resistor should be used with DTμL 944. With external R to 5 volt V_{CC} ±0.5V subtract output loads as follows:

R = 2KΩ	2 loads
R = 1KΩ	4 loads
R = 510Ω	8 loads

10 LEAD TO-5 PACKAGE



DTμL 930 DUAL GATE
DTμL 932
DUAL BUFFER
DTμL 944
DUAL POWER GATE

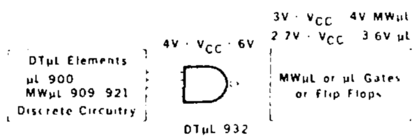
MISCELLANEOUS APPLICATIONS

NOTE [illegible]

INTERFACING

[illegible] 12 volts. Line Receiver may have nominal low level [illegible] nominal threshold ≅ 4V and nominal high level [illegible] 8V. [illegible] Resistor selected should be as low as possible [illegible] number of [illegible] and power dissipation of system. For a guaranteed V_{OH} level above [illegible], an I_{VCE} selection may be desirable. [illegible] resistor that requires the 944 to sink more than 40 mA [illegible] V_{OL} above .40 volt), a high current I_{OL} - V_{OL} selection may be desirable.

DRIVING μL AND MWμL

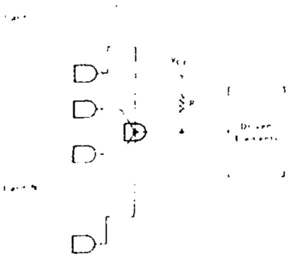


Rules: With V_{CC} 4.5V a 932 will drive 25 unit Logic loads or 100 MWμL unit loads.

Derate DTμL output drive by 25% for DTμL 932 V_{CC} = 4 V.

Refer to DTμL 932 Output Current vs. Output Voltage curve, Page 3, for matching to μL-MWμL [illegible] requirements.

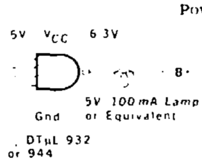
POWER GATING



Each output driver is 1/2 DTμL 944. Note that the DTμL 944 is a direct high fan-out replacement for DTμL 930, except that an external resistor must be used.

LAMP DRIVING

Suggested Ratings T_A 75°C
Power Dissipation TO-5 400mW Maximum
Power Dissipation Cerpak 240mW Maximum



Maximum "hot" lamp current:

120 mA TO-5	one side only ON
100 mA Cerpak	one side only ON
90 mA TO-5	both sides ON
75 mA Cerpak	both sides ON

[illegible] 290 [illegible] 250 mA

[illegible] 932 or 944

TO-5 Package 50 msec Cerpak 100 msec

[illegible]

[redacted]

SC08853 (4-4)

Figure A-8. Fairchild DTμL 932 and DTμL 944 (Sheet 4 of 4)

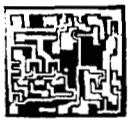
MOTOROLA Semiconductors

BOX 955 • PHOENIX, ARIZONA 85001

MC1533

MONOLITHIC
SILICON EPITAXIAL PASSIVATED

JANUARY 1967 — DS 9060 R1
Replaces DS 9060



. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

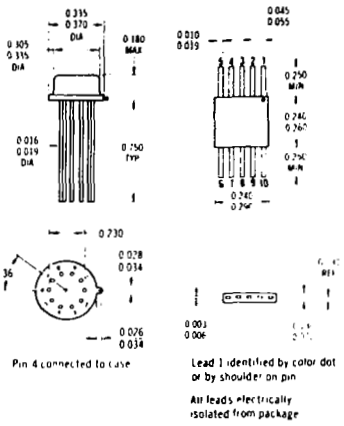
- High-Performance Open Loop Gain Characteristics
  A_{VOL} = 60,000 typical
- Low Temperature Drift — ±5 μV/°C
- Large Output Voltage Swing —
  ±13 V typical @ ±15 V Supply
- Low Output Impedance — Z_{out} = 100 ohms typical
- Input Offset Voltage Adjustable to Zero

Characteristic	Symbol	Rating	Unit
Power Supply Voltage	V^+ V^-	+20 -20	Vdc Vdc
Differential Input Signal	V_{in}	±10	Volts
Common Mode Input Swing	CMV_{in}	±V^+	Volts
Load Current	I_L	10	mA
Output Short Circuit Duration	I_S	1.0	s
Power Dissipation (Package Limitation) Metal Can Derate above T_A = 25°C Flat Package Derate above T_A = 25°C	P_D	 680 4.6 500 3.3	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

(TO-91)

10-PIN METAL CAN
G SUFFIX

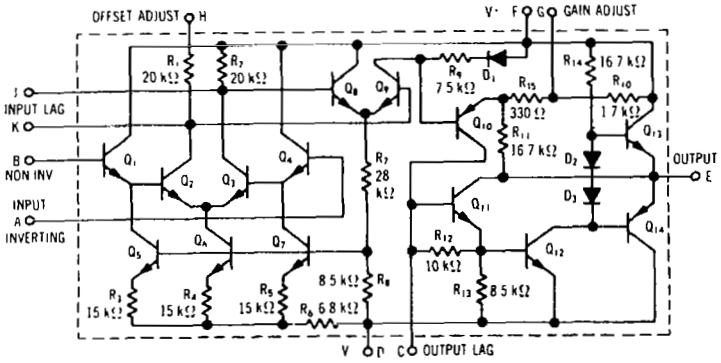
10-PIN FLAT PACKAGE
F SUFFIX



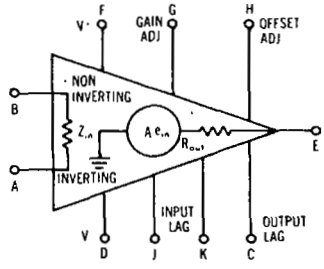
PIN CONNECTIONS

Schematic	A	B	C	D	E	F	G	H	J	K
"G" Package	1	2	3	4	5	6	7	8	9	10
"F" Package	10	1	2	3	4	5	6	7	8	9

CIRCUIT SCHEMATICS



CIRCUIT SCHEMATIC



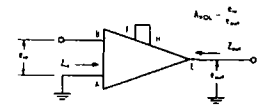
EQUIVALENT CIRCUIT

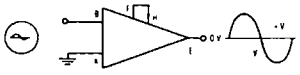
SC08857 (1-4)

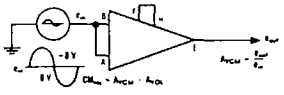
LINEAR INTEGRATED CIRCUIT
MC1533
DS 9060 R1

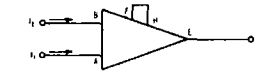
Figure A-9. Motorola MC1533 (Sheet 1 of 4)

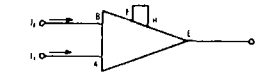
Characteristic Definitions①

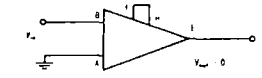


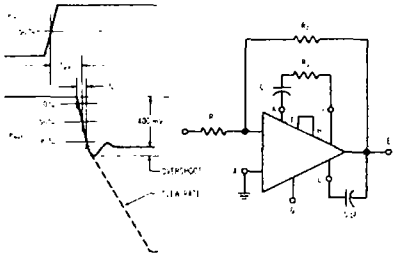


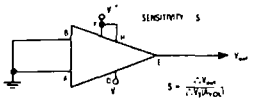












Characteristic	Symbol	Min	Typ	Max	Unit
Open Loop Voltage Gain	A_{VOL}				-
(V @ Pin G = +15 Vdc)		40,000	60,000	120,000	
(Pin G open)		15,000	30,000	45,000	
(V@ Pin G = +15 Vdc, T_A = -55 C, +125 C)		35,000	50,000	120,000	
(Pin G open, T_A = -55 C, +125 C)		12,000	25,000	45,000	
Output Impedance	Z_{out}				Ω
(Pin G open, f = 20 Hz)		-	100	150	
Input Impedance	Z_{in}				kΩ
(Pin G open, f = 20 Hz)		500	1000	-	
Output Voltage Swing	V_{out}				V_{peak}
(R_L = 10 kΩ)		±12	±13	-	
(R_L = 2 kΩ)		±11	±12	-	
Input Common Mode Voltage Swing	CMV_{in}	+9	+10	-	V_{peak}
		-8	-9	-	
Common Mode Rejection Ratio	CM_{rej}				dB
(V @ Pin G = +15 Vdc)		90	100	-	
(Pin G open)		80	94	-	
Input Bias Current	I_b				μA
$\left(I_b = \frac{I_1 + I_2}{2}\right)$ (T_A = +25°C)		-	0.5	1.0	
(T_A = -55 C, +125 C)		-	-	3.0	
Input Offset Current	I_{io}				μA
($I_{io} = I_1 - I_2$)		-	0.03	0.15	
($I_{io} = I_1 - I_2$, T_A = -55 C)		-	-	0.5	
($I_{io} = I_1 - I_2$, T_A = +125 C)		-	-	0.2	
Input Offset Voltage ②	V_{io}				mV
(T_A = 25°C)		-	1.0	5.0	
(T_A = -55 C, +125 C)		-	-	6.0	
Step Response					
Gain = 100, 15% overshoot,	t_r	-	0.15		μs
R_1 = 1 kΩ, R_2 = 100 kΩ,	t_{pd}	-	0.06	-	μs
R_3 = 100 Ω, C_1 = 0.02 μF	dV_{out}/dt ③	-	11.0	-	V/μs
Gain = 10, no overshoot,	t_r	-	0.3	-	μs
R_1 = 1 kΩ, R_2 = 10 kΩ,	t_{pd}	-	0.1	-	μs
R_3 = 10 Ω, C_1 = 0.05 μF	dV_{out}/dt ③	-	1.5	-	V/μs
Gain = 1, 20% overshoot,	t_r	-	0.2	-	μs
R_1 = 10 kΩ, R_2 = 10 kΩ,	t_{pd}	-	0.3	-	μs
R_3 = 5 Ω, C_1 = 0.1 μF	dV_{out}/dt ③	-	0.6	-	V/μs
Average Temperature Coefficient of Input Offset Voltage	$TC_{V_{io}}$				μV/°C
(T_A = -55 C to +25 C)		-	8.0	-	
(T_A = +25°C to +125 C)		-	5.0	-	
Average Temperature Coefficient of Input Offset Current	$TC_{I_{io}}$				nA/°C
(T_A = -55 C to +125 C)		-	0.1	-	
(T_A = +25°C to +125 C)		-	0.05	-	
DC Power Dissipation	P_D				mW
(Power Supply = ±15 V, V_{out} = 0)		-	120	170	
Positive Supply Sensitivity	S^+				μV/V
(V^+ constant)		-	50	150	
Negative Supply Sensitivity	S^-				μV/V
(V^- constant)		-	50	150	

① All definitions imply linear operation

② Input offset voltage (V_{io}) may be adjusted to zero by varying the potential on pin H

③ dV_{out}/dt = Slew Rate

SC08857 (2-4)

Figure A-10. Motorola MC1533 (Sheet 2 of 4)

TYPICAL CHARACTERISTICS

FIGURE 6 POWER DISSIPATION versus POWER SUPPLY VOLTAGE

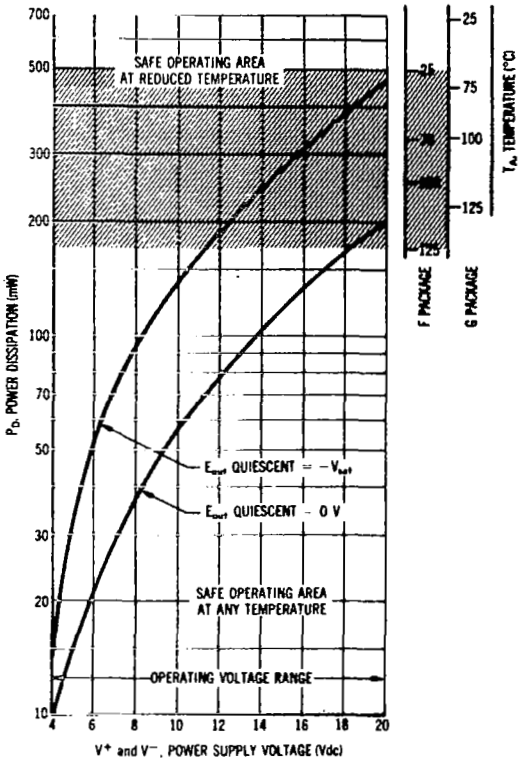


FIGURE 7 VOLTAGE GAIN versus POWER SUPPLY VOLTAGE

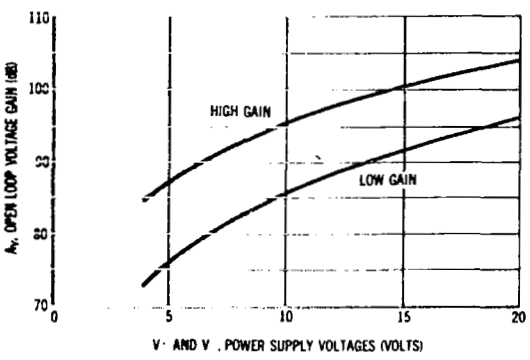


FIGURE 8 COMMON MODE SWING versus POWER SUPPLY VOLTAGE

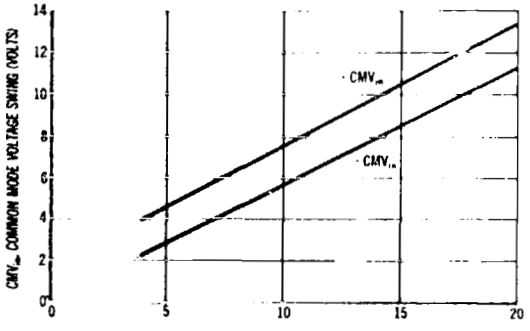


FIGURE 9 INPUT OFFSET VOLTAGE versus TEMPERATURE

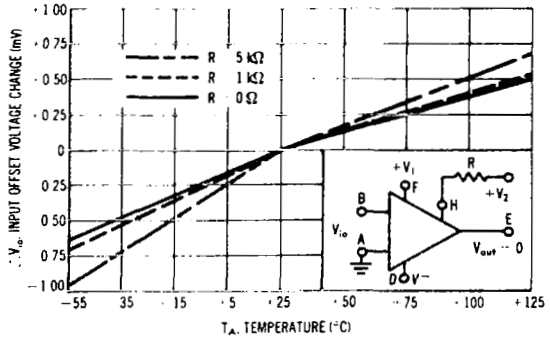
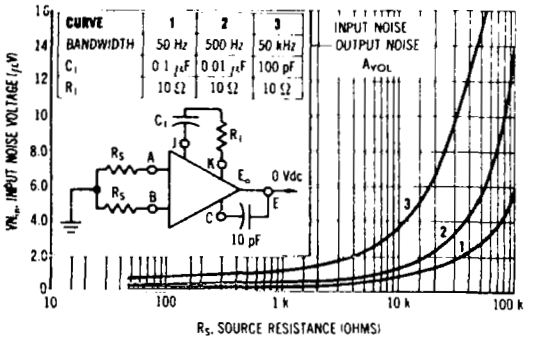


FIGURE 10 INPUT NOISE VOLTAGE versus SOURCE RESISTANCE

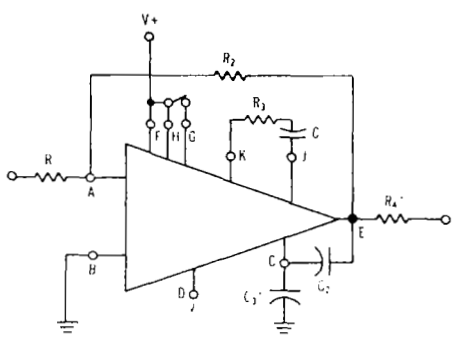


SC08857 (4-4)

MOTOROLA Semiconductor Products Inc.
BOX 955 • PHOENIX ARIZONA 85001 • A SUBSIDIARY OF MOTOROLA INC

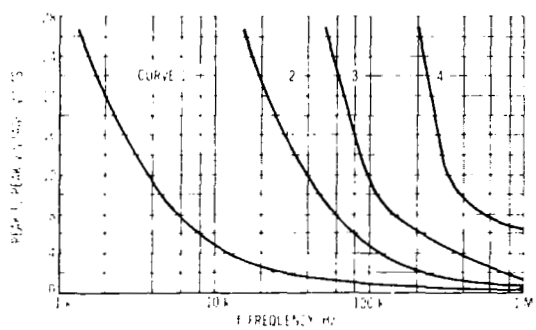
Figure A-11. Motorola MC1533 (Sheet 3 of 4)

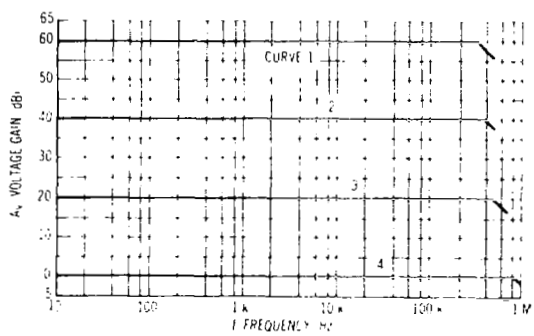
V -15 Vdc V 15 Vdc T_A 25 C

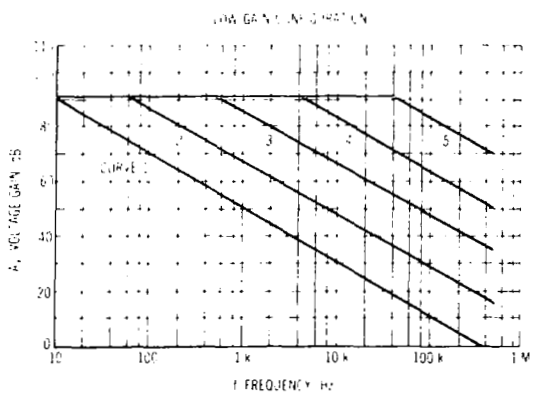


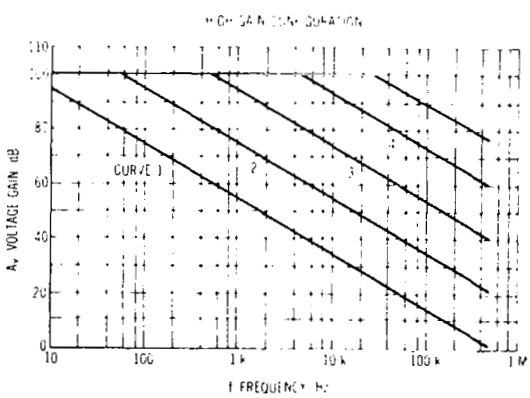
FOR CAPACITIVE LOADS R_4 47 Ω OR C_3 47 pF

Fig. No.	Curve No.	Test Conditions R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	C_1	C_2 (pF)	C_3 (pF)
2	1	10k	10k	5	1 μF	10	47
	2	10k	100k	10	0.1 μF	10	47
	3	1k	1M	510	820 pF	10	47
	3	10k	1M	100	0.05 μF	10	47
	4	1k	1M	100	0.05 μF	3	47
	4	1k	1M	510	820 pF	3	47
3	1 (Low Gain)	1k	1M	10	1000 pF	10	47
	1 (High Gain)	1k	1M	510	820 pF	10	47
	2 (Low Gain)	10k	1M	10	0.01 μF	10	47
	2 (High Gain)	10k	1M	100	0.01 μF	10	47
	3 (Low Gain)	10k	100k	10	0.1 μF	10	47
	3 (High Gain)	10k	100k	10	0.1 μF	10	47
	4 (Low Gain)	10k	10k	10	1 μF	10	47
	4 (High Gain)	10k	10k	5	1 μF	10	47
4	1	0	∞	10	1 μF	10	47
	2	0	∞	10	0.1 μF	10	47
	3	0	∞	10	0.01 μF	10	47
	4	0	∞	10	1000 pF	10	47
	5	0	∞	10	100 pF	10	47
5	1	∞	∞	10	1 μF	10	47
	2	∞	∞	10	0.1 μF	10	47
	3	∞	∞	10	0.01 μF	10	47
	4	∞	∞	10	1000 pF	10	47
	5	∞	∞	10	100 pF	10	47









SC08857 (3-4)

Figure A-12. Motorola MC1533 (Sheet 4 of 4)

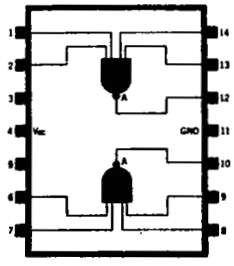
LOW POWER MONOLITHIC TTL ELEMENT

DUAL NAND/NOR GATE DRIVER

SE455J

AUGUST 1966

The SE455J is a semiconductor integrated circuit fabricated within a monolithic substrate by planar and epitaxial techniques. It was designed for maximum speed consistent with extremely low power operation. It is intended for use in applications where high density packaging and the ability to drive high capacitances associated with multilayer printed-circuit boards are important considerations. The SE455J offers two buffer/driver elements in the TO-88, 14 lead flat package. It is compatible with the other elements of the SE400J series under worst-case temperature and power supply variation.

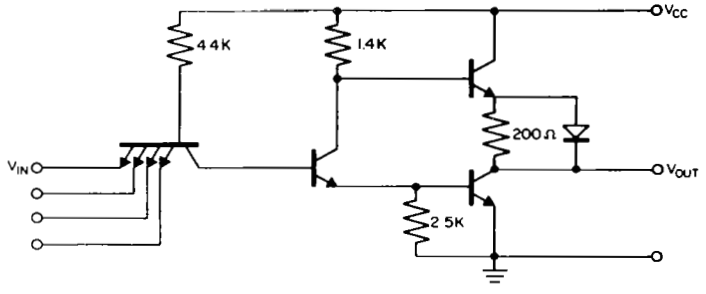


NOTE:
(1) A—Active pull-up

FEATURES

• LOW POWER	7.0 mW
• HIGH NOISE IMMUNITY	1.0 volt
• HIGH FAN-OUT	28
• HIGH SPEED	28 ns/Gate
• BROAD TEMPERATURE RANGE	−55°C to +125°C

BASIC CIRCUIT SCHEMATIC

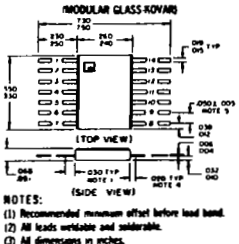


NOTE: ½ of SE455J shown. Component values are typical

PERFORMANCE GUARANTEE NOTICE

This data sheet is a complete procurement document for the product described. Noise margins, speed, and fan-out are guaranteed from −55°C to +125°C over a broad range of power supply and temperature differentials between driving and driven units. In addition to presenting guarantees immediately applicable by system designers, the needs of component and reliability engineers are met by full details of the quality assurance and reliability programs that stand behind the guarantees. Acceptance Test Sub-Groups called out in the tabular data refer to selection and test criteria as specified in Table II of SURE Program Bulletin No. 5001.

J-PACKAGE—(TO-88)



NOTES:
(1) Recommended minimum offset before lead bend.
(2) All leads weldable and solderable.
(3) All dimensions in inches.
(4) Lead spacing dimensions apply in this area only.
(5) Spacing tolerances non-cumulative

SE455J

SC08861 (1-6)

SIGNETICS CORPORATION • 811 EAST ARQUES AVENUE, SUNNYVALE CALIFORNIA • TEL: (408) 739-7700 • TWX: (910) 339-9220

Figure A-13. Signetics SE455J (Sheet 1 of 6)

SE455J

This data sheet has two sections The first section is a specification table of guaranteed test limits The second section is a set of general information characteristic curves

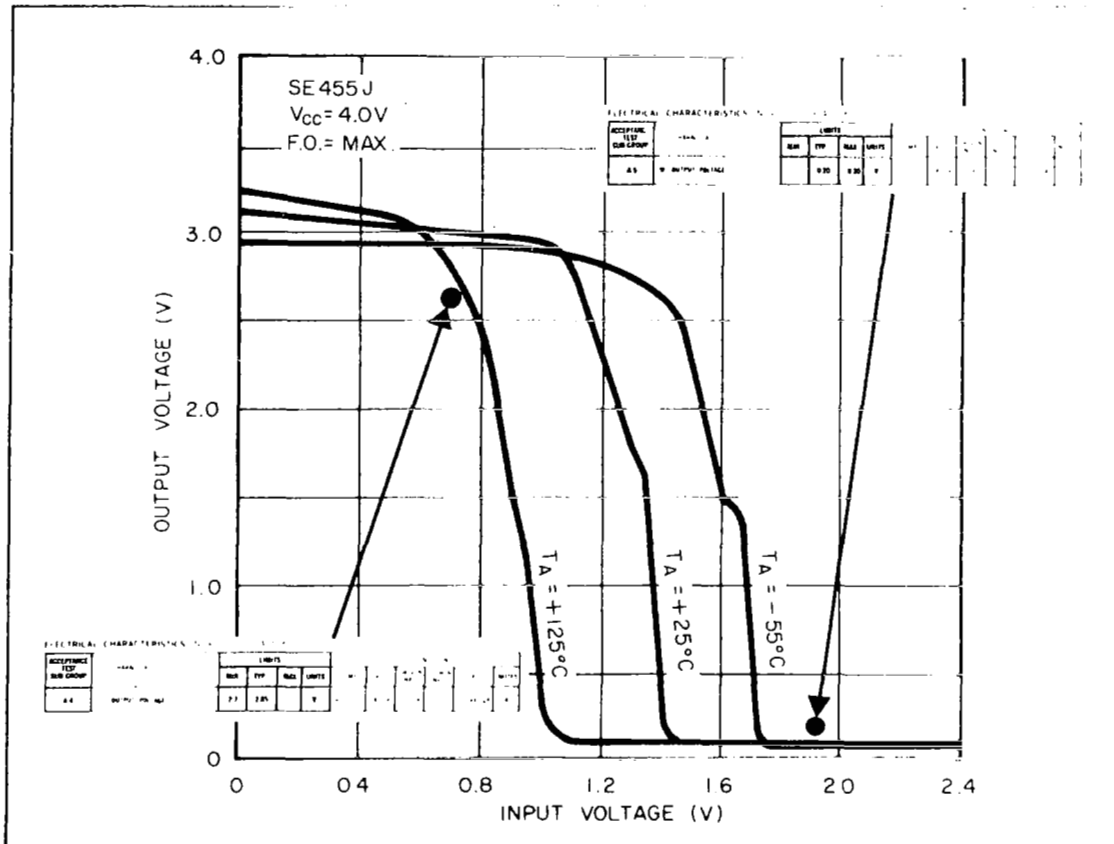
The test limit tables contain a set of parameter test points that are guaranteed by SIGNETICS under the SURE Testing Program The test points guaranteed cover a broad range of parameters under varying conditions of power supply voltage, loading conditions and environments

The characteristic curve data are intended to provide the designer with meaningful system design limits over a broader range of operating conditions than do the test limit tables

The curves are derived from devices selected to assure a high probability that the units used in your system will function well within the design limits you may establish from the characteristic curve data For the designer who wishes to have characteristic curve points guaranteed, special test points may be established for an additional charge In most cases, special test point guarantees will be negotiated plus or minus a tolerance from the curve data to take into account test equipment limitations Please contact your local SIGNETICS Sales Engineer to discuss special test limit requirements

Figure 1 depicts graphically the relationship between the test limit tables and the curve data

FIGURE 1



The data presented in the guaranteed test limit table may be interrelated to determine other meaningful information For instance, the 1 DCM or noise margin may be calculated for worst case conditions by taking the difference between the minimum "1" output voltage and the minimum "1" input voltage at the worst case temperature and power supply to be encountered in the system For the "0" DCM or noise margin, calculate the difference between the maximum "0" input voltage and maximum "0" output voltage

SC08861 (2-6)

Figure A-14. Signetics SE455J (Sheet 2 of 6)

SECTION 1

ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 4, 5, 6)

ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS					
		MIN.	TYP.	MAX.	UNITS	TEMP.	V	DRIVEN INPUT	OTHER INPUTS	OUTPUTS	NOTES
A-5	"1" OUTPUT VOLTAGE	2.7	2.85		V	−55°C	4.0 V	0.9 V		−500 µA	8
A-3		2.7	2.85		V	+25°C	4.0 V	0.9 V		−500 µA	8
A-4		2.7	2.85		V	+125°C	4.0 V	0.7 V		−500 µA	8
C-1		2.3	2.45		V	−55°C	3.6 V	0.9 V		−500 µA	8
C-1		2.3	2.45		V	+25°C	3.6 V	0.9 V		−500 µA	8
C-1		2.3	2.45		V	+125°C	3.6 V	0.7 V		−500 µA	8
C-1		3.1	3.3		V	−55°C	4.4 V	0.9 V		−500 µA	8
C-1		3.1	3.3		V	+25°C	4.4 V	0.9 V		−500 µA	8
C-1		3.1	3.3		V	+125°C	4.4 V	0.7 V		−500 µA	8
A-5	"0" OUTPUT VOLTAGE		0.20	0.30	V	−55°C	4.0 V	1.9 V	1.9 V	16.0 mA	
A-3			0.25	0.30	V	+25°C	4.0 V	1.7 V	1.7 V	16.0 mA	
A-4			0.25	0.30	V	+125°C	4.0 V	1.3 V	1.3 V	16.0 mA	
C-1			0.20	0.30	V	−55°C	3.6 V	1.9 V	1.9 V	12.0 mA	
C-1				0.30	V	+125°C	3.6 V	1.3 V	1.3 V	16.0 mA	
C-1			0.20	0.30	V	−55°C	4.4 V	1.9 V	1.9 V	18.0 mA	
C-1			0.25	0.30	V	+125°C	4.4 V	1.3 V	1.3 V	16.0 mA	
C-1	"0" INPUT CURRENT			−0.84	mA	−55°C	4.0 V	0.3 V	4.0 V		
A-3		−0.50	−0.65	−0.85	mA	+25°C	4.0 V	0.3 V	4.0 V		
C-1				−0.84	mA	+125°C	4.0 V	0.3 V	4.0 V		
C-1			−0.55	−0.75	mA	+25°C	3.6 V	0.3 V	4.0 V		
C-1			−0.80	−0.96	mA	+25°C	4.4 V	0.3 V	4.0 V		
A-3	"1" INPUT CURRENT			10.0	µA	+25°C	4.0 V	3.6 V	0 V		
A-4				20.0	µA	+125°C	4.0 V	3.6 V	0 V		
A-6	PAIR DELAY	40	55	85	nsec	+25°C	4.0 V			DC F.O. 22	9
C-2	(Fig. 2)	45	58	95	nsec	+25°C	3.6 V			DC F.O. 22	9
C-2		35	52	85	nsec	+25°C	4.4 V			DC F.O. 22	9
C-2	OUTPUT FALL TIME		15	20	nsec	+25°C	4.0 V			AC F.O. 8	10
A-6	(Fig. 3)		60	75	nsec	−55°C	3.6 V			AC F.O. 8	10
C-2	INPUT CAPACITANCE			3.0	pf	+25°C	4.0 V	2.0 V			7
	POWER CONSUMPTION (Per Gate)										
A-4	OUTPUT "0"		12.5	15.6	mW	+125°C	4.0 V				
C-1	OUTPUT "0"		10.0	13.3	mW	+125°C	3.6 V				
C-1	OUTPUT "0"		15.5	19.3	mW	+125°C	4.4 V				
A-2	OUTPUT "1"		3.0	4.0	mW	+25°C	4.0 V	0 V			
C-1	OUTPUT "1"		2.5	3.3	mW	+25°C	3.6 V	0 V			
C-1	OUTPUT "1"		4.0	5.3	mW	+25°C	4.4 V	0 V			
A-2	INPUT VOLTAGE RATING	6.0			V	+25°C	4.0 V	50 µA			
A-2	OUTPUT SHORT CIRCUIT CURRENT	−20		−80	mA	+25°C	4.0 V	0 V		0 V	

NOTES

(1) All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.

(2) All measurements are taken with Pin 11 tied to zero volts.

(3) Positive current flow is defined as into the terminal referenced.

(4) Positive NAND logic definition: UP = Level 1, DOWN = Level 0.

(5) *Precautionary measures should be taken to insure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.*

(6) Measurements apply to each gate element independently.

(7) Capacitance as measured on *Boonton Electronic Corporation Model 75A-SB* Capacitance Bridge or equivalent, f = 1 MHz, V = 25 mV. All pins not specifically referenced are tied to guard for capacitance tests.

(8) Output leakage current is supplied through a resistor to ground.

(9) D.C. Fan out is defined in terms of a SIGNETICS Standard Unit Load which is an SE480J gate input or an equivalent impedance.

(10) *One AC Fan out is defined as equivalent to one clock pulse input of an SE4731 or a 50 pf capacitance load.*

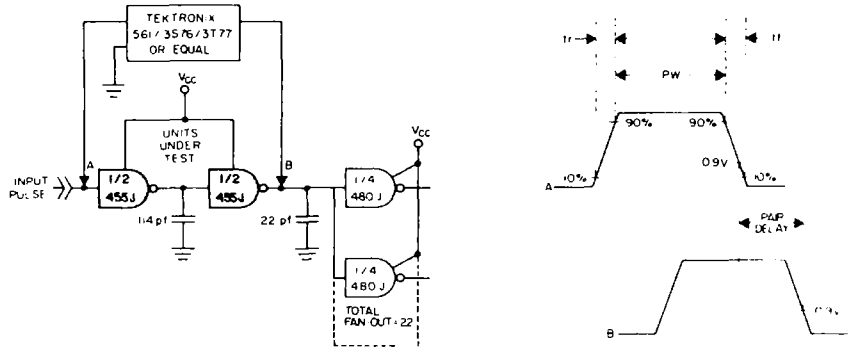
SC08861 (3-6)

Figure A-15. Signetics SE455J (Sheet 3 of 6)

SE455J DUAL NAND/NOR GATE DRIVER

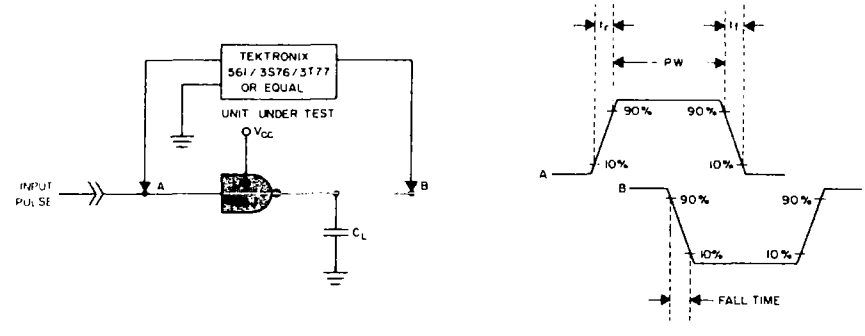
SECTION 1

FIGURE 2 — PAIR DELAY



NOTES (1) Capacitance values shown include probe and test fixture capacitance
(2) Input Pulse Characteristics Amplitude 2.7 V, f 1.0 MHz, PW 350 ns, t t 10 ns

FIGURE 3 — FALL TIME



NOTES (1) C includes test fixture and probe capacitance C 462 pf for fan out of 8 and 77 pf for fan out of 1
(2) Input Pulse Characteristics Amplitude 2.7 V, f 1.0 MHz, PW 200 ns, t t 10 ns

ABSOLUTE MAXIMUM RATINGS:

INPUT VOLTAGE	6.0 V	OPERATING TEMP.	−55°C to +125°C
V_{CC}	6.0 V	STORAGE TEMP.	−65°C to +175°C
INPUT CURRENT	±10 mA	$()_{J\text{-}A}$ (R_{TH} Junction to Still Air)	0.3°C/mW
OUTPUT CURRENT	±100 mA	JUNCTION TEMP.	175°C MAX.

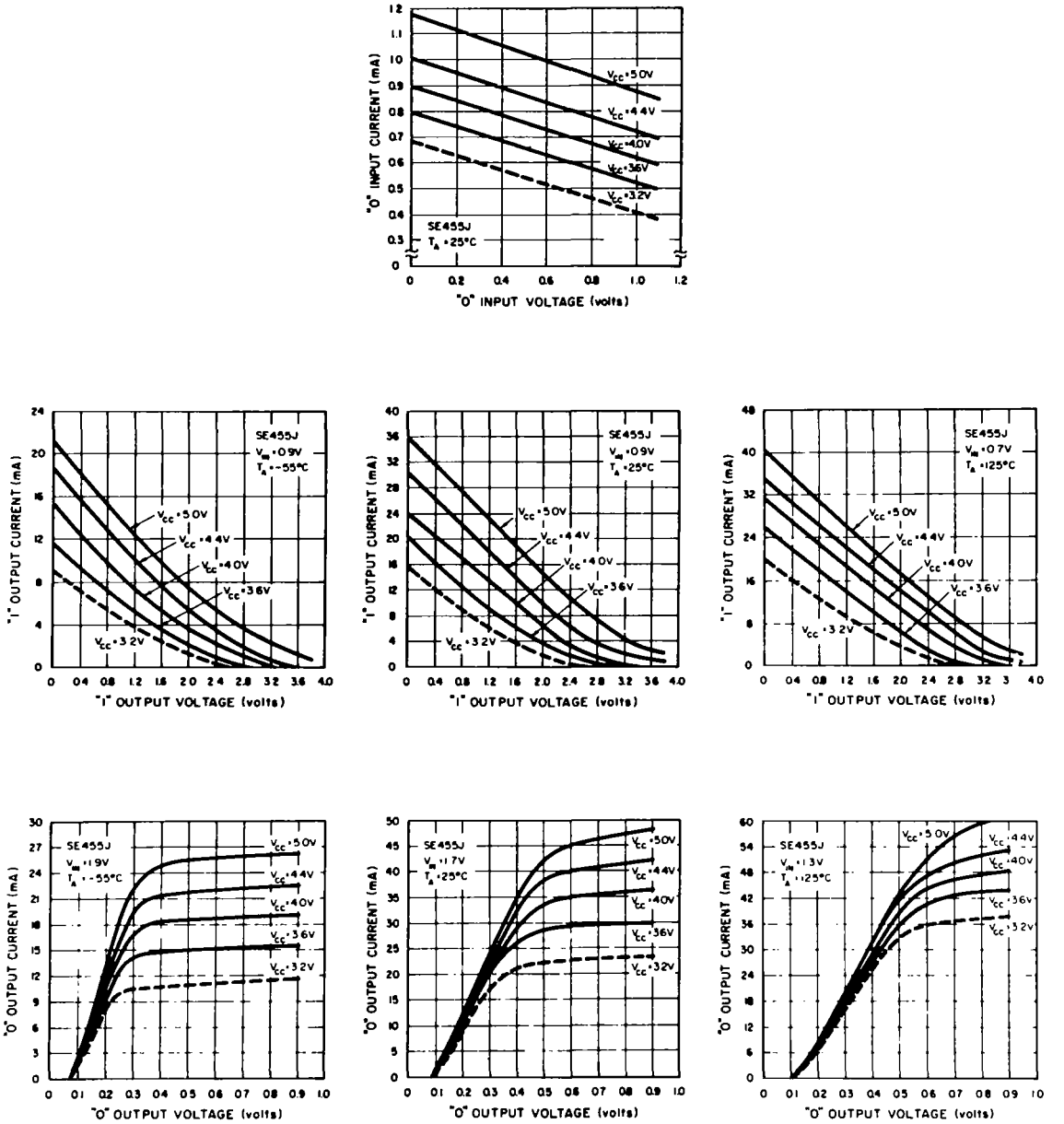
Maximum ratings are limiting values above which serviceability may be impaired

SC08861 (4-6)

Figure A-16. Signetics SE455J (Sheet 4 of 6)

SE455J DUAL NAND/NOR GATE DRIVER

SECTION 2 — SYSTEM DESIGN LIMIT CURVES

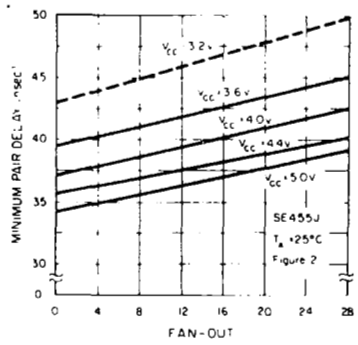


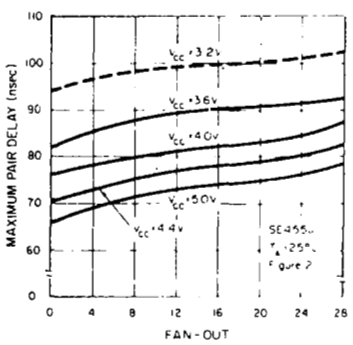
SC08861 (5-6)

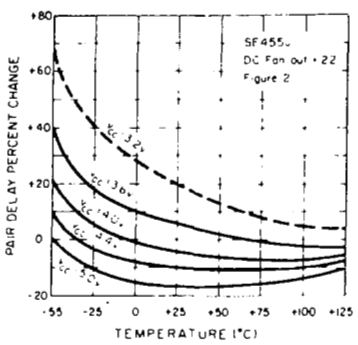
Figure A-17. Signetics SE455J (Sheet 5 of 6)

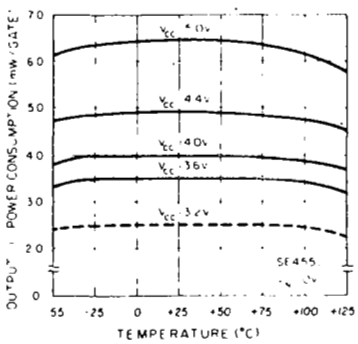
SE455J DUAL NAND/NOR GATE DRIVER

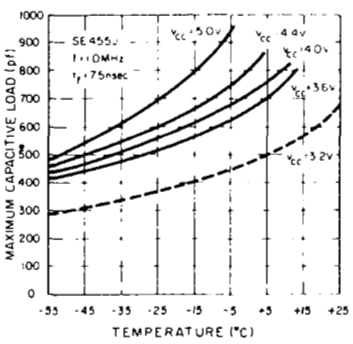
SECTION 2 — SYSTEM DESIGN LIMIT CURVES



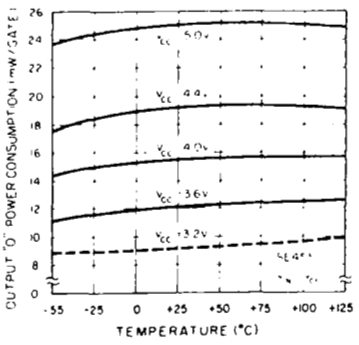


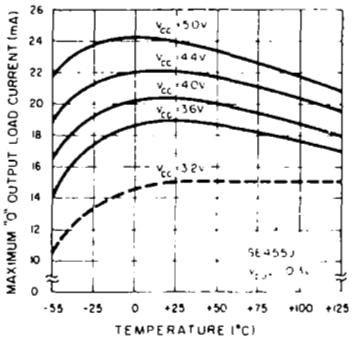






"Maximum Capacitive Load vs T_A" depicts AC fan out capability for the SE455J in terms of capacitance driven when the output fall time is restricted to 75 ns maximum. One AC fan out is defined as equivalent to one clock input of an SE424J (50 pf maximum). The SE424J clock input pulse fall time should not exceed 75 ns. Since AC fan-out is limited to 8 under worst case conditions, the curve only extends to 25°C.





"Maximum "0" Output Load Current vs T_A" depicts DC fan out in terms of output current sinking capability. DC fan-out may be derived by determining the output current capability under the appropriate conditions from the curve and dividing by the appropriate Input "0" Current for the driven element.

SC08861 (6-6)

SIGNETICS CORPORATION • 811 EAST ARQUES AVENUE; SUNNYVALE CALIFORNIA • TEL: (408) 739-7700 • TWX: (910) 339-9220

Figure A-18. Signetics SE455J (Sheet 6 of 6)

SOLID CIRCUIT®
SEMICONDUCTOR NETWORKS†

TYPE SN523A
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPE SN523A
BULLETIN NO. DL-S 646494, MARCH 1964
REPLACES ENGINEERING SPEC. DATED AUGUST 1964

SERIES 52 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER
for application as

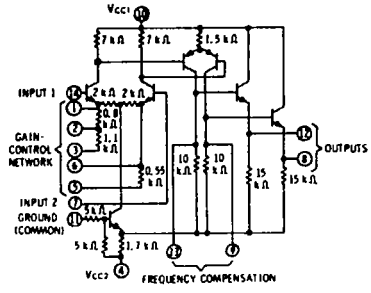
- **Comparator**
- **Level Detector**
- **Differential Amplifier**
- **Voltage Regulator**

- **Military & Industrial Control Systems**
- **Analog-to-Digital Converters**
- **Analog Computers**

description

The SN523A, offering differential inputs and differential emitter-follower outputs, incorporates a resistance network in the emitters of the input stage to facilitate gain adjustment. From the wide range of total resistance available, a particular value may be selected by connecting the resistor-network pins in a configuration which produces the desired gain. Maximum-gain configuration is with pin ① shorted to pin ⑥.

The SN523A, one of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.
SCHEMATIC DIAGRAM

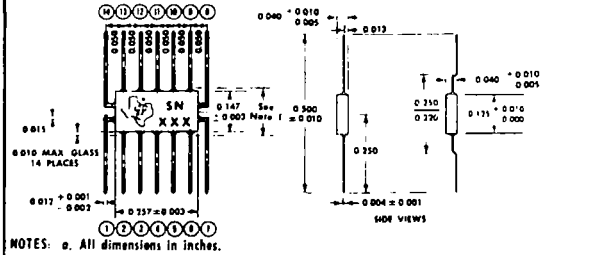
mechanical data

The SN523A is mounted in a glass-to-metal hermetically sealed welded package meeting TO-84. Leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN523A is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

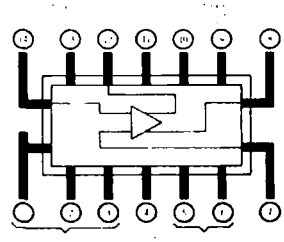
ORDERING INSTRUCTIONS

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



NOTES: a. All dimensions in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing tolerance is ±0.015 at extremities and ±0.005 at package, noncumulative.
d. Lead centerlines are located within ±0.005 of their true positions relative to body centerlines.
e. Overall dimensions of package and glass meniscus can be held to 0.155 by special request.
f. Symbolization denotes orientation of package.



†Patented by Texas Instruments

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 24% nickel, and 17% cobalt.

SC08867 (1-4)

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

Figure A-19. Texas Instruments SN523A (Sheet 1 of 4)

TYPE SN523A
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): V_{CC1} . . . . . +15 V
V_{CC2} . . . . . −15 V
Differential Input Voltage . . . . . ±6 V
Input Voltage (Either Input, See Note 1) . . . . . ±10 V
Duration of Short-Circuit Output Current . . . . . 5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2) . . . . . 300 mW
Operating Free-Air Temperature Range . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.
2. Derate linearly to 120 mW at 125°C free-air temperature at the rate of 1.8 mW/deg.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage			2.2	12	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	T_A = −55°C to 125°C		9		μV/deg
V_{CMO}	Common-mode output offset voltage			500		mV
I_{in}	Input current			5		μA
I_{DI}	Differential-input offset current			0.5	2	μA
V_{OM}	Maximum peak-to-peak output voltage	Differential output, f = 1 kc/s		24		V
		Differential output, f = 1 kc/s, T_A = −55°C to 125°C	20			V
V_{CMIM}	Maximum common-mode input voltage			±5		V
A_{VD}	Differential voltage gain	f = 1 kc/s		4000		
		f = 1 kc/s, T_A = −55°C to 125°C	2500			
		f = 1 kc/s, pins ① and ④ open		135		
		f = 1 kc/s, pin ① shorted to pin ⑨, pin ④ open		830		
		f = 1 kc/s, pin ② shorted to pin ⑤, pins ① and ④ open		465		
		f = 1 kc/s, pin ③ shorted to pin ⑤, pins ① and ④ open		325		
		f = 1 kc/s, pin ③ shorted to pin ⑧, pin ① open		680		
CMRR	Common-mode rejection ratio	f = 1 kc/s		90		dB
BW	Bandwidth (−3 dB)		70	180		kc/s
Z_{in}	Input impedance	f = 1 kc/s	5	15		kΩ
Z_{out}	Output impedance	f = 1 kc/s		200		Ω
P_T	Total power dissipation			100		mW

§Unless otherwise noted, test conditions are:
V_{CC1} = +12 V, V_{CC2} = −12 V, V_{DI} applied, no external loading; pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ⑦, ⑩, ⑤, ⑨ and ⑪ open.

letter symbol and parameter definitions

V_{DI} — That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.
V_{CMO} — That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.
I_{in} — The current into either input of the amplifier.
I_{DI} — The difference in the currents into the two input terminals when the output is balanced.
V_{OM} — The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
V_{CMIM} — The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR — The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW — The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.
Z_{in} — The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
Z_{out} — The impedance between the output terminal and ground when the output is balanced.

SC08867 (2-4)

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

Figure A-20. Texas Instruments SN523A (Sheet 2 of 4)

TYPICAL CHARACTERISTICS§

INPUT CURRENT
vs
FREE-AIR TEMPERATURE

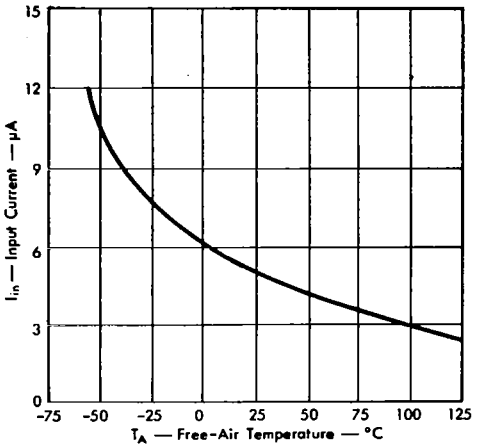


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

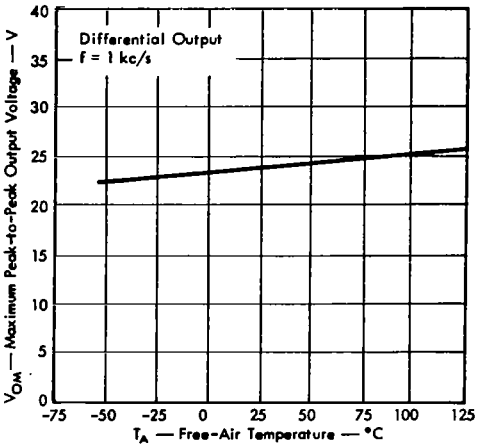


FIGURE 2

SINGLE-ENDED VOLTAGE GAIN
vs
FREQUENCY

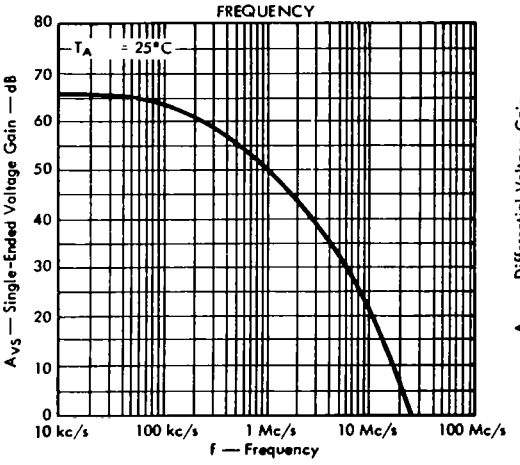


FIGURE 3

DIFFERENTIAL VOLTAGE GAIN
vs
SUPPLY VOLTAGE

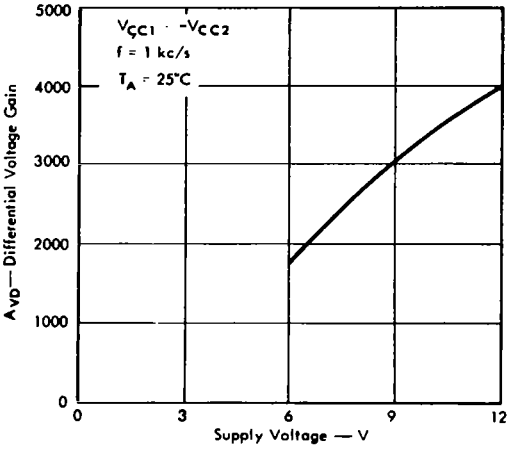


FIGURE 4

§Unless otherwise noted, test conditions are:
V_{CC1} = +12 V, V_{CC2} = −12 V, V_{D1} applied, no external loading, pin ⑪ grounded, pin ① shorted to pin ⑤, and pins ②, ③, ⑥, ⑦ and ⑩ open.

SC08867 (3-4)

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

Figure A-21. Texas Instruments SN523A (Sheet 3 of 4)

TYPE SN523A
GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

TYPICAL CHARACTERISTICS§

DIFFERENTIAL VOLTAGE GAIN
vs
FREE-AIR TEMPERATURE

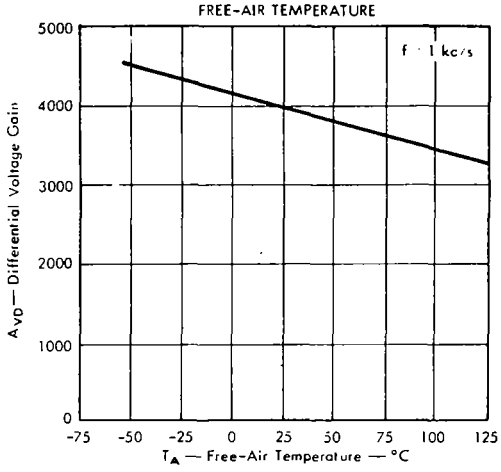


FIGURE 5

INPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

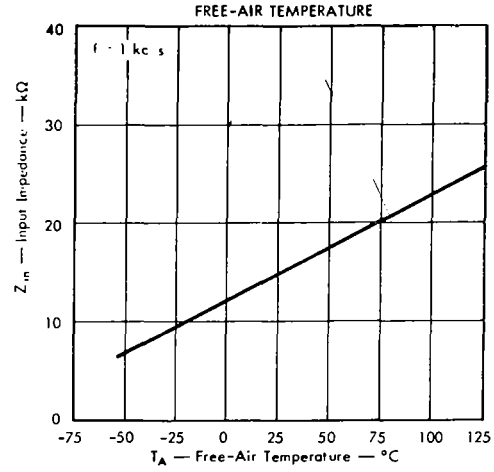


FIGURE 6

OUTPUT IMPEDANCE
vs
FREE-AIR TEMPERATURE

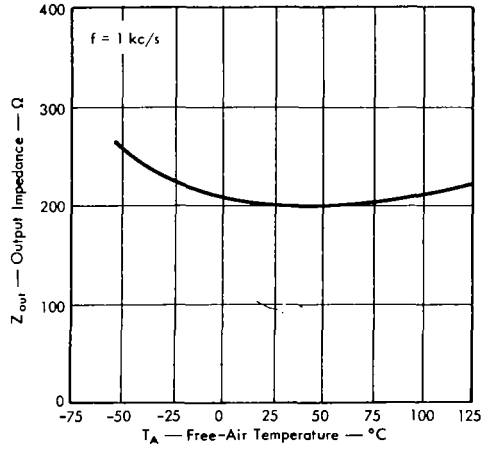


FIGURE 7

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

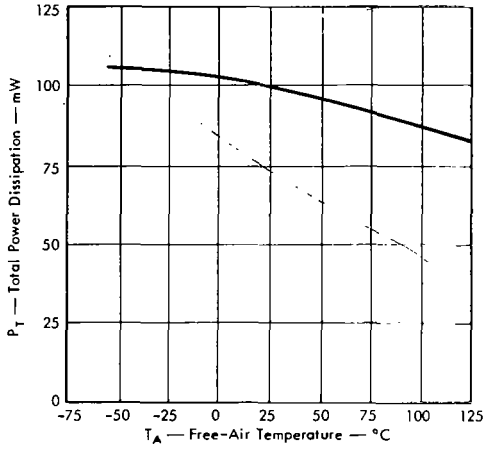


FIGURE 8

§Unless otherwise noted, test conditions are:
V_{CC1} = +12 V, V_{CC2} = −12 V, V_{DI} applied, no external loading, pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

SC08867 (4-4)

PRINTED IN U.S.A.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

Figure A-22. Texas Instruments SN523A (Sheet 4 of 4)

INTEGRATED CIRCUITS

NEW-PRODUCT BULLETIN

This announcement provides preliminary engineering information on new Texas Instruments products. Definitive specifications are now being prepared for publication.

SOLID CIRCUIT®
SEMICONDUCTOR NETWORKS†

TYPES SN52 709, SN52 709L, SN72 709, SN72 709L
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

SERIES 52/72 OPERATIONAL AMPLIFIERS

featuring

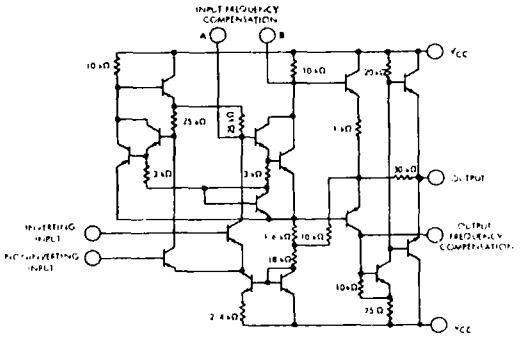
Common-Mode Input Range — ±10 V

Peak-to-Peak Output Voltage Swing — ±14 V

description

The SN52 709 circuit is a high-performance operational amplifier with high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces an amplifier with low drift and offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly attractive for applications requiring transfer or generation of linear or non-linear functions. The SN52 709 and SN52 709L are characterized for operation over the temperature range of -55°C to 125°C. The SN72 709 and SN72 709L are characterized for operation from 0°C to 70°C.

Texas Instruments Series 52/72 catalog lines of linear integrated circuits offer higher reliability, lower cost, smaller size, and less weight than equivalent discrete component circuits.

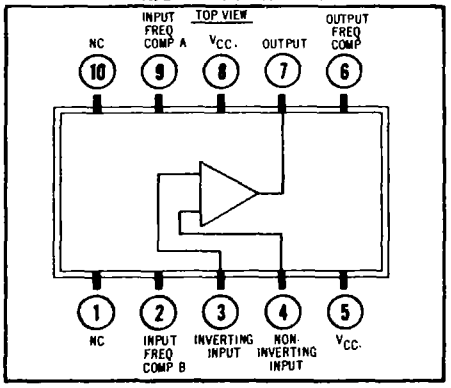


Component values shown are nominal.

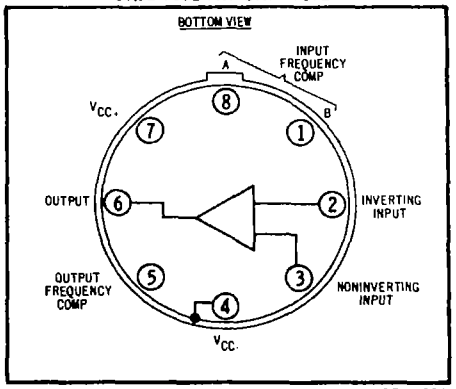
SCHEMATIC DIAGRAM

TERMINAL ASSIGNMENTS

SN52 709 and SN72 709



SN52 709L and SN72 709L



NC — No internal connection

†Patented by Texas Instruments.

SC08871 (1-4)

SC 9420A
DECEMBER 1966
REPLACES SC 9420 NOVEMBER 1966

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

PRINT

Figure A-23. Texas Instruments SN52709 (Sheet 1 of 4)

TYPES SN52 709, SN52 709L
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

absolute maximum ratings

Supply Voltages (See Note 1): V_{CC+}	+18 V
V_{CC-}	-18 V
Differential Input Voltage	±5 V
Input Voltage (Either Input, See Note 1)	±10 V
Duration of Short-Circuit Output Current (T_A = 25°C)	5 s
Continuous Total Power Dissipation: SN52 709L (See Note 2)	300 mW
SN52 709 (See Note 3)	250 mW
Operating Temperature Range (See Notes 2 and 3)	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C

NOTES: 1. These voltage values are with respect to the zero reference level of the supply voltage.
2. At free-air temperature (T_A) above 95°C derate power dissipation linearly at 5.6 mW/deg.
3. At case temperature (T_C) above 100°C derate power dissipation linearly at 5 mW/deg.

electrical characteristics (unless otherwise noted, V_{CC+} = 15 V and V_{CC-} = -15 V, to V_{CC+} = 9 V and V_{CC-} = -9 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage	$R_S \leq 10$ kΩ, T_A = -55°C to 125°C			6	mV
		$R_S \leq 10$ kΩ		1	5	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	R_S = 50 Ω, T_A = -55°C to 125°C		3		μV/deg
		$R_S \leq 10$ kΩ, T_A = -55°C to 125°C		6		μV/deg
I_{DI}	Differential-input offset current	T_A = 125°C		20	200	nA
				50	200	nA
		T_A = -55°C		100	500	nA
I_{in}	Input Current			200	500	nA
		T_A = -55°C		500	1500	nA
V_{OM}	Maximum peak-to-peak output voltage	V_{CC+} = 15 V, V_{CC-} = -15V, $R_L \geq 10$ kΩ, T_A = -55°C to 125°C	±12	±14		V
		V_{CC+} = 15 V, V_{CC-} = -15 V, $R_L \geq 2$ kΩ, T_A = -55°C to 125°C	±10	±13		V
V_{CMI}	Common-mode input voltage range	V_{CC+} = 15 V, V_{CC-} = -15 V, T_A = -55°C to 125°C	±8	±10		V
A_V	Large-signal voltage gain	V_{CC+} = 15 V, V_{CC-} = -15 V, $R_L \geq 2$ kΩ, V_{out} = ±10 V, T_A = -55°C to 125°	25,000	45,000	70,000	
CMRR	Common-mode rejection ratio	$R_S \leq 10$ kΩ, T_A = -55°C to 125°C	70	90		dB
SVRR	Supply voltage rejection ratio	$R_S \leq 10$ kΩ, T_A = -55°C to 125°C		25	150	μV/V
r_{in}	Input resistance	T_A = -55°C to 125°C	40	100		kΩ
			150	400		kΩ
r_{out}	Output resistance			150		Ω
P_T	Total power dissipation	V_{CC+} = 15 V, V_{CC-} = -15 V		80	165	mW

transient response, V_{CC+} = 15 V and V_{CC-} = -15 V, to V_{CC+} = 9 V and V_{CC-} = -9 V, T_A = 25°C (See Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_{in} = 20 mV, C_L = open		0.3	1	μs
	Overshoot	V_{in} = 20 mV, $C_L \leq 100$ pF		10	30	%

SC08871 (2-4)

Figure A-24. Texas Instruments SN52709 (Sheet 2 of 4)

absolute maximum ratings

Supply Voltages (See Note 1): V_{CC+}	+18 V
V_{CC-}	−18 V
Differential Input Voltage	±5 V
Input Voltage (Either Input, See Note 1)	±10 V
Duration of Short-Circuit Output Current (T_A = 25°C)	5 s
Continuous Total Power Dissipation: SN72 709L (See Note 4)	250 mW
SN72 709 (See Note 5)	250 mW
Operating Free-Air Temperature Range (See Notes 4 and 5)	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. These voltage values are with respect to the zero reference level of the supply voltage.
4. At free-air temperature (T_A) above 55°C derate power dissipation linearly at 5.6 mW/deg.
5. At case temperature (T_C) above 100°C derate power dissipation linearly at 5 mW/deg.

electrical characteristics V_{CC+} = 15 V and V_{CC-} = −15 V, (unless otherwise noted, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage	$R_S \le 10$ kΩ, T_A = 0°C to 70°C (See Note 6)			10	mV
		$R_S \le 10$ kΩ (See Note 6)		2	7.5	mV
I_{DI}	Differential-input offset current	T_A = 0°C to 70°C			750	nA
				100	500	nA
I_{in}	Input current	T_A = 0°C			2	μA
				0.3	1.5	μA
V_{OM}	Maximum peak-to-peak output voltage	$R_L \ge 10$ kΩ	±12	±14		V
		$R_L \ge 2$ kΩ	±10	±13		V
V_{CMI}	Common-mode input voltage range		±8	±10		V
A_V	Large-signal voltage gain	$R_L \ge 2$ kΩ, V_{out} = ±10 V, T_A = 0°C to 70°C	12,000			
		$R_L \ge 2$ kΩ, V_{out} = ±10 V	15,000	45,000		
CMRR	Common-mode rejection ratio	$R_S \le 10$ kΩ	65	90		dB
SVRR	Supply voltage rejection ratio	$R_S \le 10$ kΩ		25	200	μV/V
r_{in}	Input resistance		50	250		kΩ
r_{out}	Output resistance			150		Ω
P_T	Total power dissipation			80	200	mW

NOTE 6: V_{CC+} = 15 V and V_{CC-} = −15 V to V_{CC+} = 9 V and V_{CC-} = −9 V.

TRANSIENT RESPONSE TEST CIRCUIT FOR SN52 709L AND SN52 709

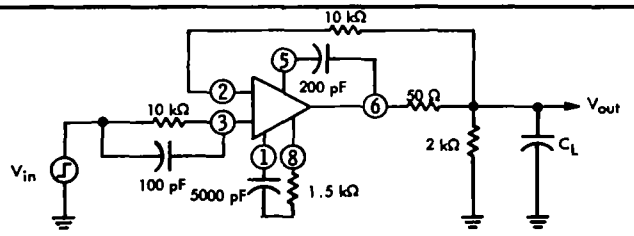


FIGURE 1

SC08871 (3-4)

Figure A-25. Texas Instruments SN52709 (Sheet 3 of 4)

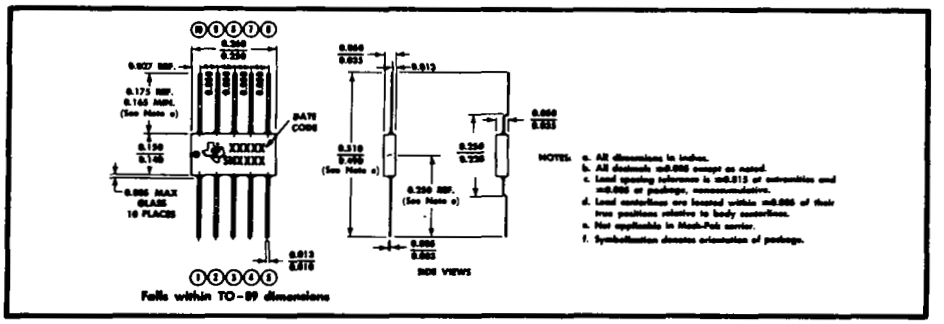
TYPES SN52 709, SN52 709L, SN72 709, SN72 709L
HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

mechanical data

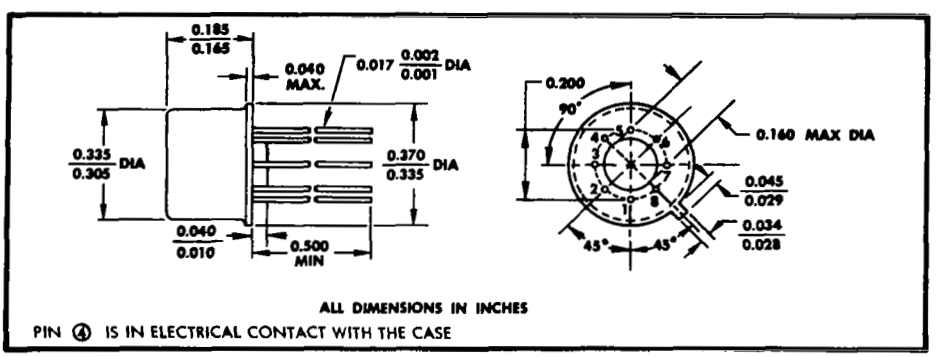
The SN52 709 and SN72 709 amplifiers are mounted in glass-to-metal hermetically sealed welded packages meeting TO-89. Leads are gold-plated F-15† glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. Both are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

ORDERING INSTRUCTIONS

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



The SN52 709L and SN72 709L package outlines are same as JEDEC TO-99 except for diameter of standoff.



† F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

SC08871 (4-4)

Figure A-26. Texas Instruments SN52709 (Sheet 4 of 4)

INDEX

NASA-Langley, 1969 — 9